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Debugging IP Router Subsystems-- Logic Analysis Tools for POS, Gigabit Ethernet and ATM

September 21, 2001

presented by:

Scott Ferguson

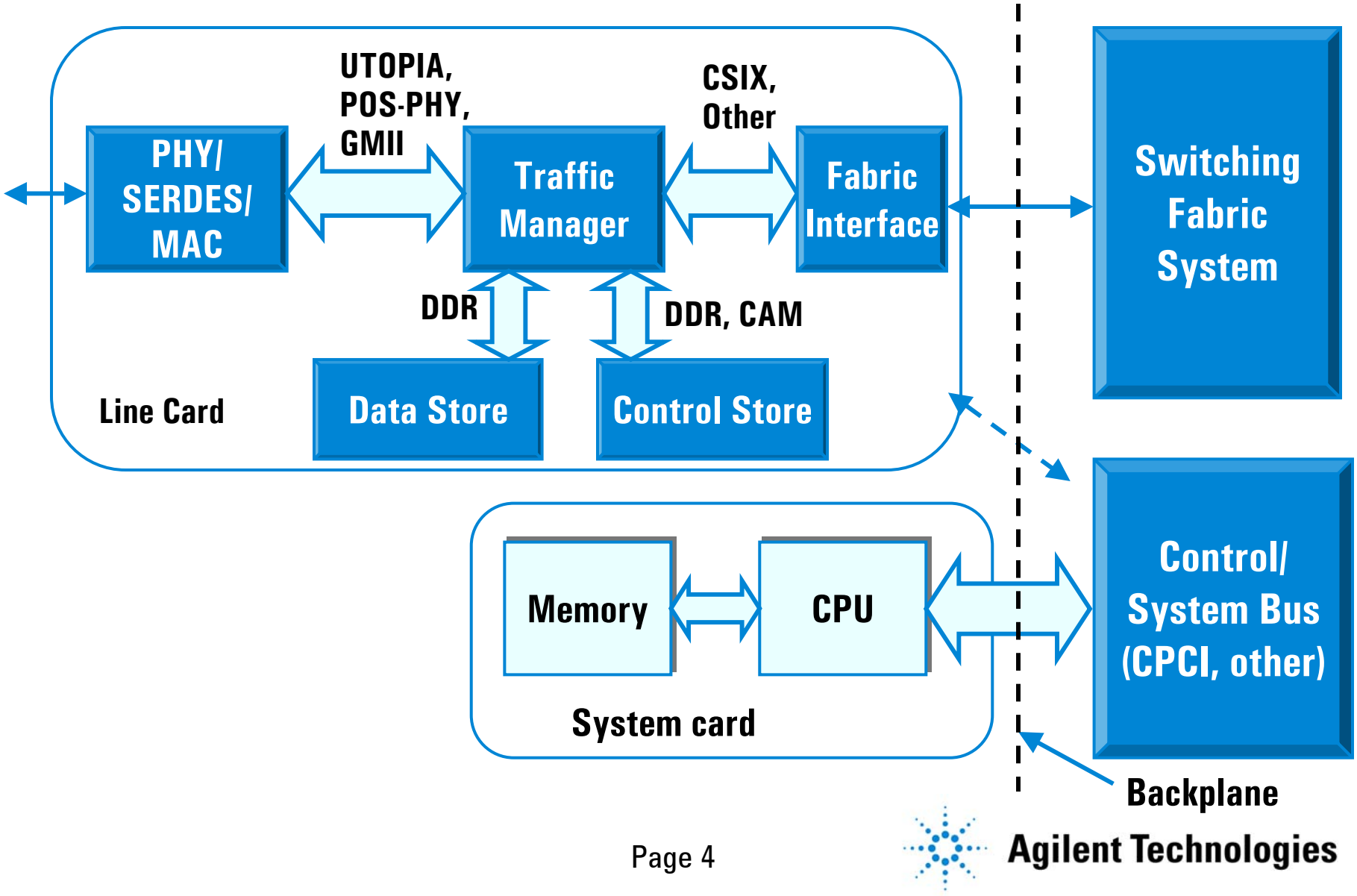
Agenda

- Overview of router architecture & subsystems
- Designing in testability
- Example problems & solutions
- Conclusion and summary

Bandwidth Demand Fuels Competition

- Highest (compliant) performance wins
  - Speed
  - Throughput
  - Intelligent response to dynamic environment
- Time to market is key

Sample Router Architecture



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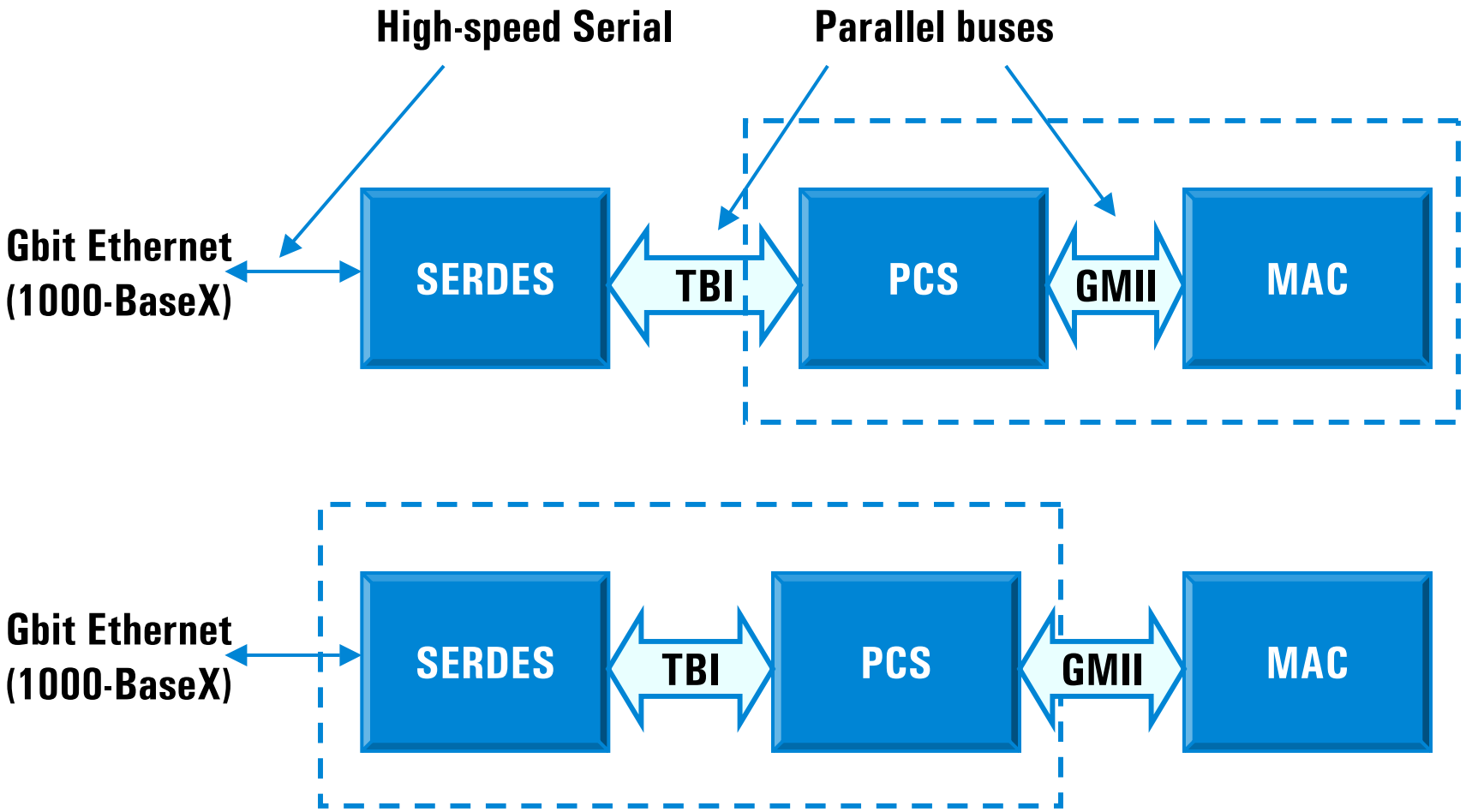
PHY Buses & Integration



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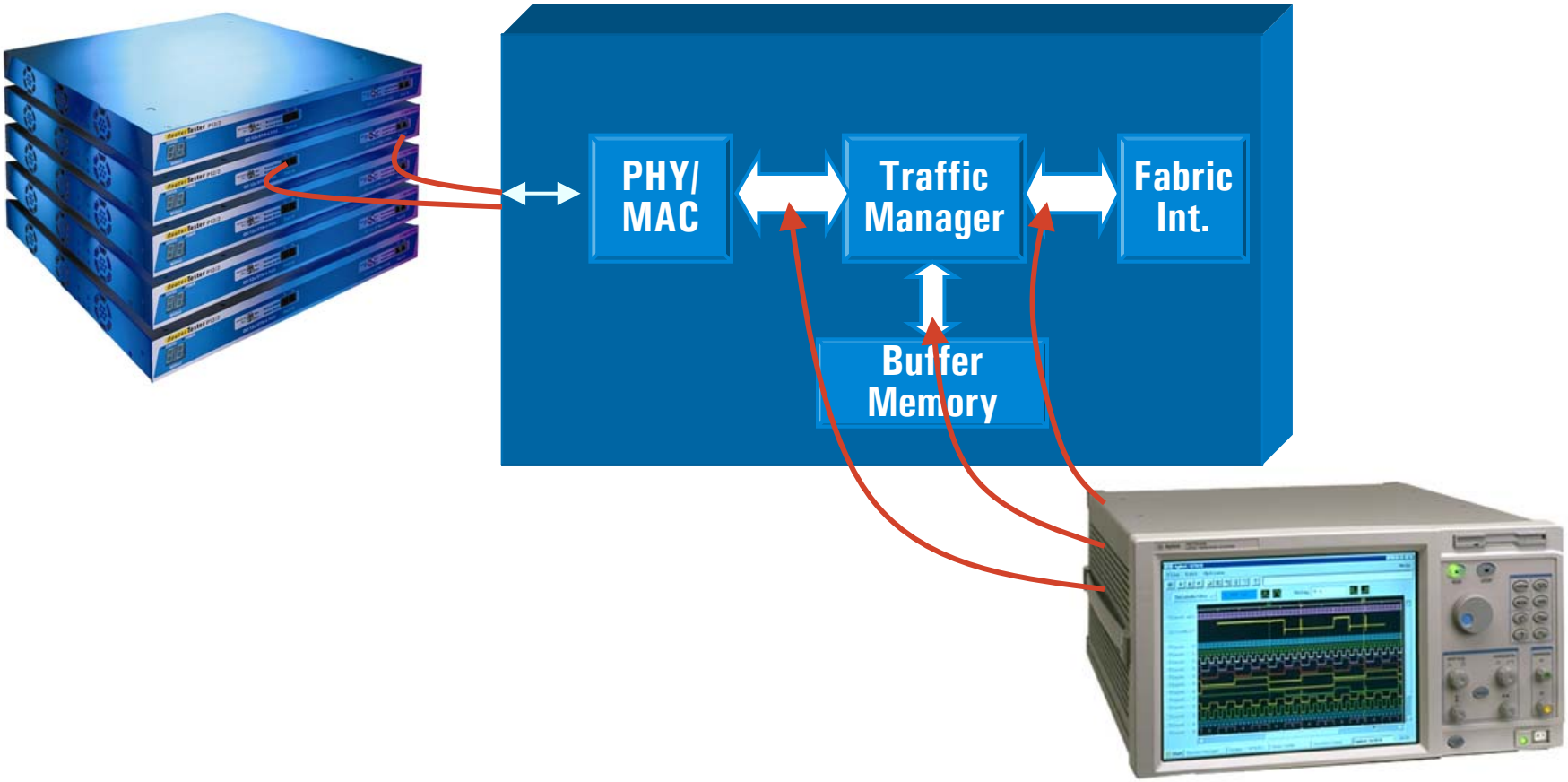
Debugging Subsystems



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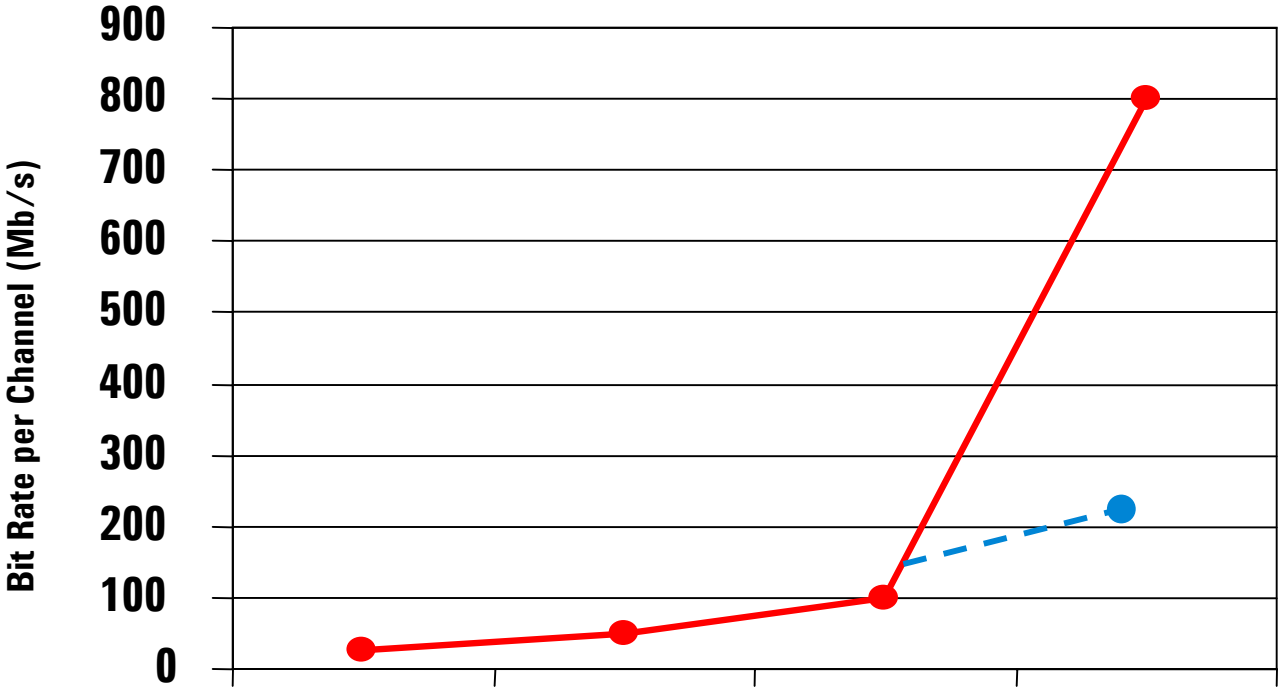
LVDS Breaks the Rules



	OC-3	OC-12	OC-48	OC-192
Line Rate	155 Mb/s	622 Mb/s	2.5 Gb/s	10 Gb/s
Bus Width	8 bits	16 bits	32 bits	16 bits (diff. pairs)
Channel Bit Rate	25 MHz	50 MHz	100 MHz	800 Mb/s (400 MHz)

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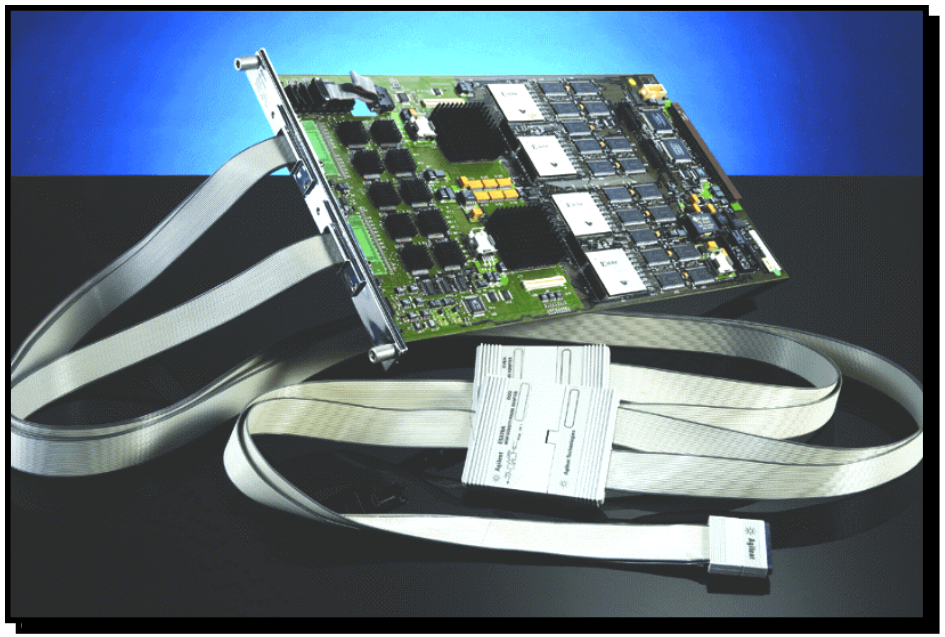
New Logic Analysis Tools

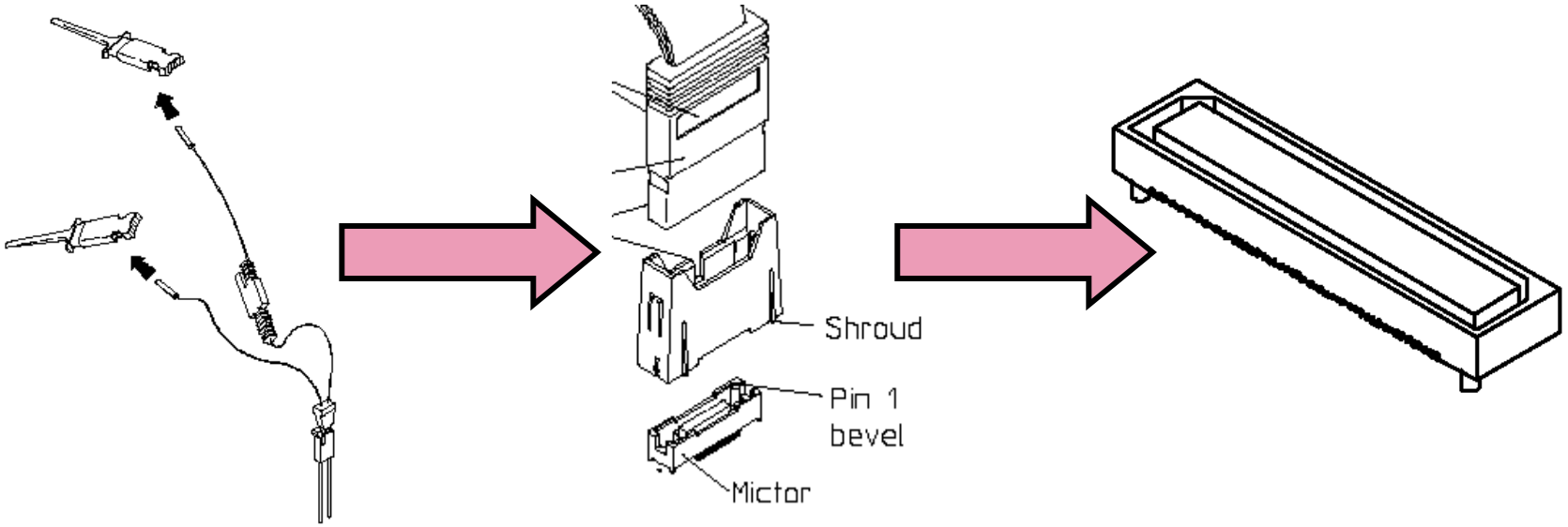
- **New 16760 state/timing module captures LVDS signals at up to 1.25 Gb/s (1.5 Gb/s coming soon)**
  - 500ps setup/hold window
  - 10 ps setup/hold resolution
  - Eye Finder technology automatically adjusts setup/hold window position
  - 64 M sample depth, 34 channels (260 Mbytes, or 2.6 M packets @ 100 bytes/packet)
  - 200 mV sensitivity



Designing in Testability

- High speeds & LVDS create probing problems
- Probing must be considered before layout
  - Pay now, or pay later
- Probing changes circuit dynamics

Designing in Testability



Year	Probing Method	Connection	Maximum Speed
1973-??	Flying Leads	Clip-on	300 MHz
1990's	AMP Mictor Connector	Surface mount	600 MHz
2001	Samtec BSH Connector	Surface mount	> 2 Gb/s

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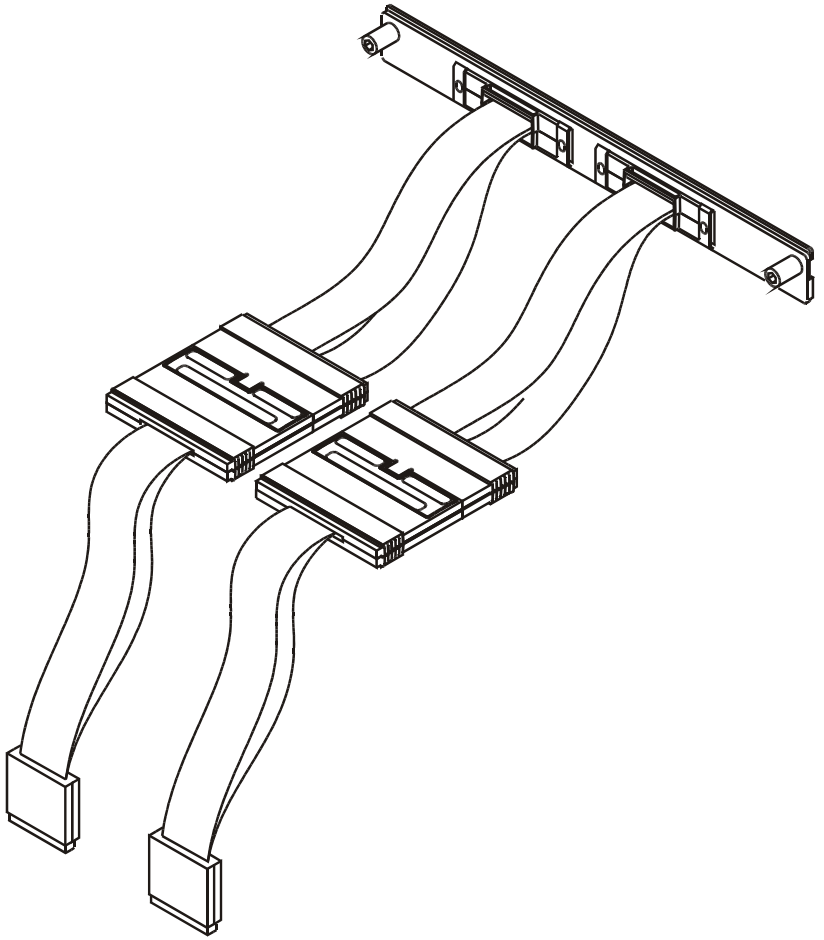
New Agilent Logic Analysis Probes

- 1.5 pF probing solution makes probing possible
- Differential probes have excellent channel-to-channel isolation at high speeds.
- Design probe connectors into target PC board



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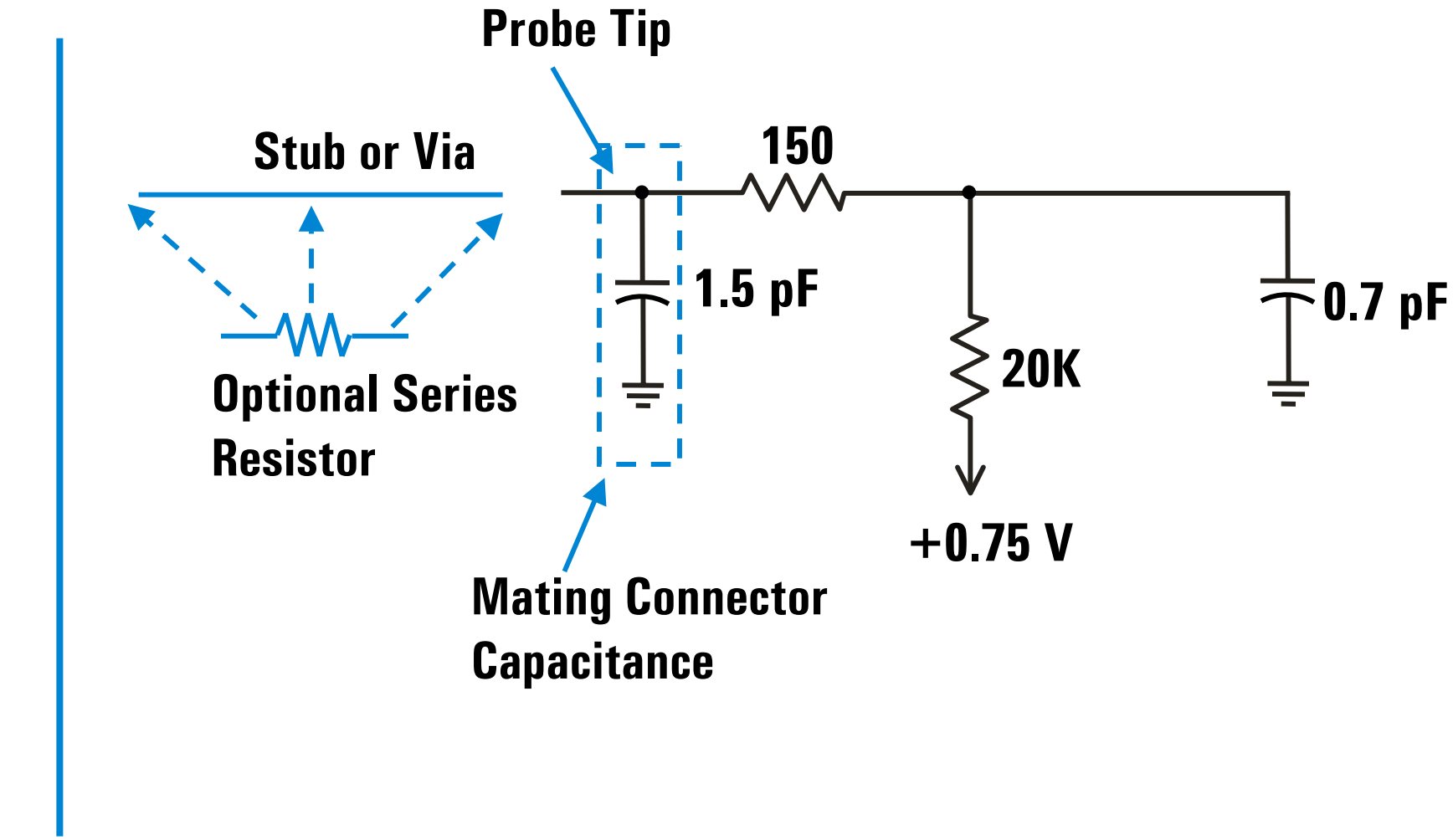
Probe Equivalent Load



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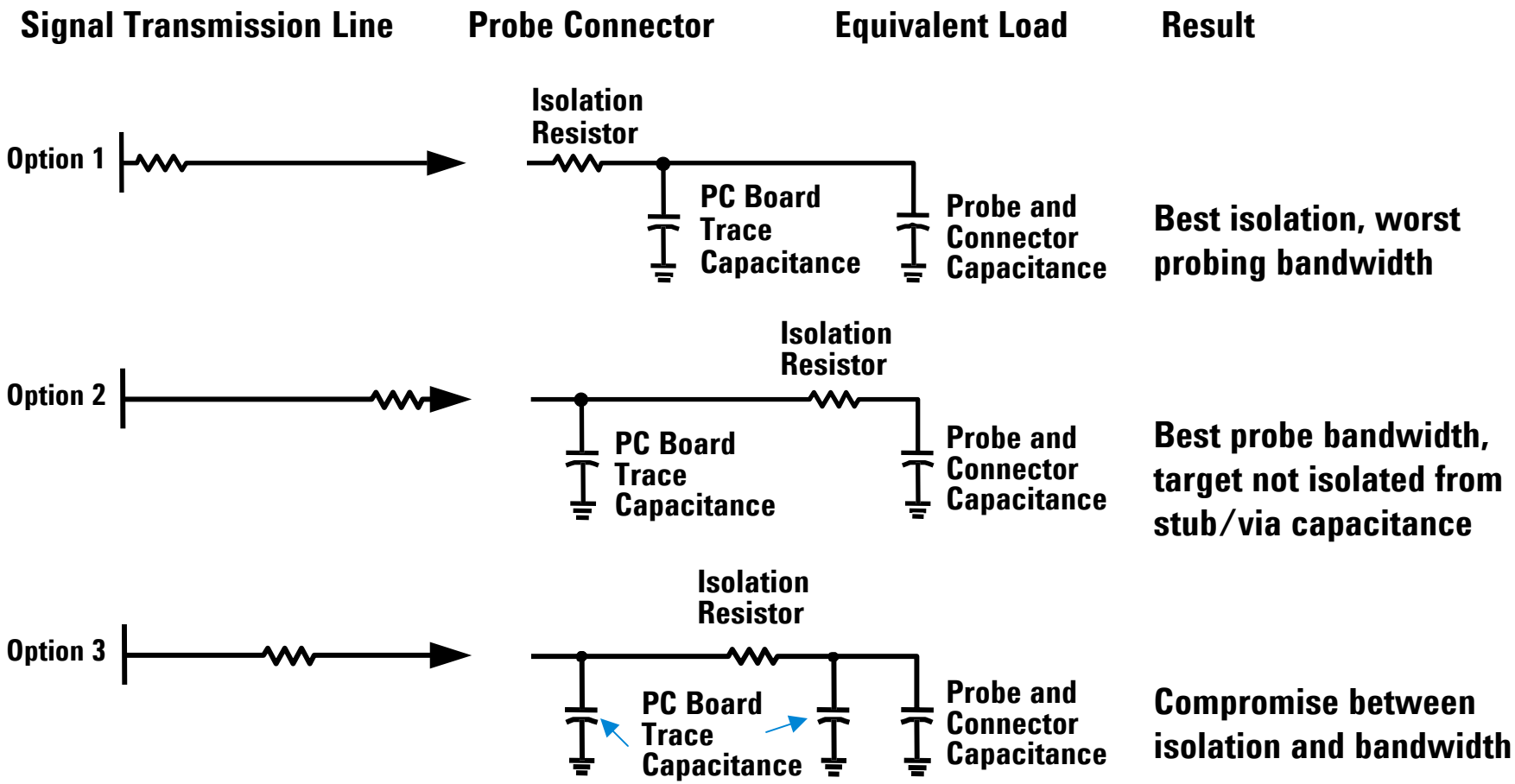
Dealing with Stubs - Adding a Series Resistor



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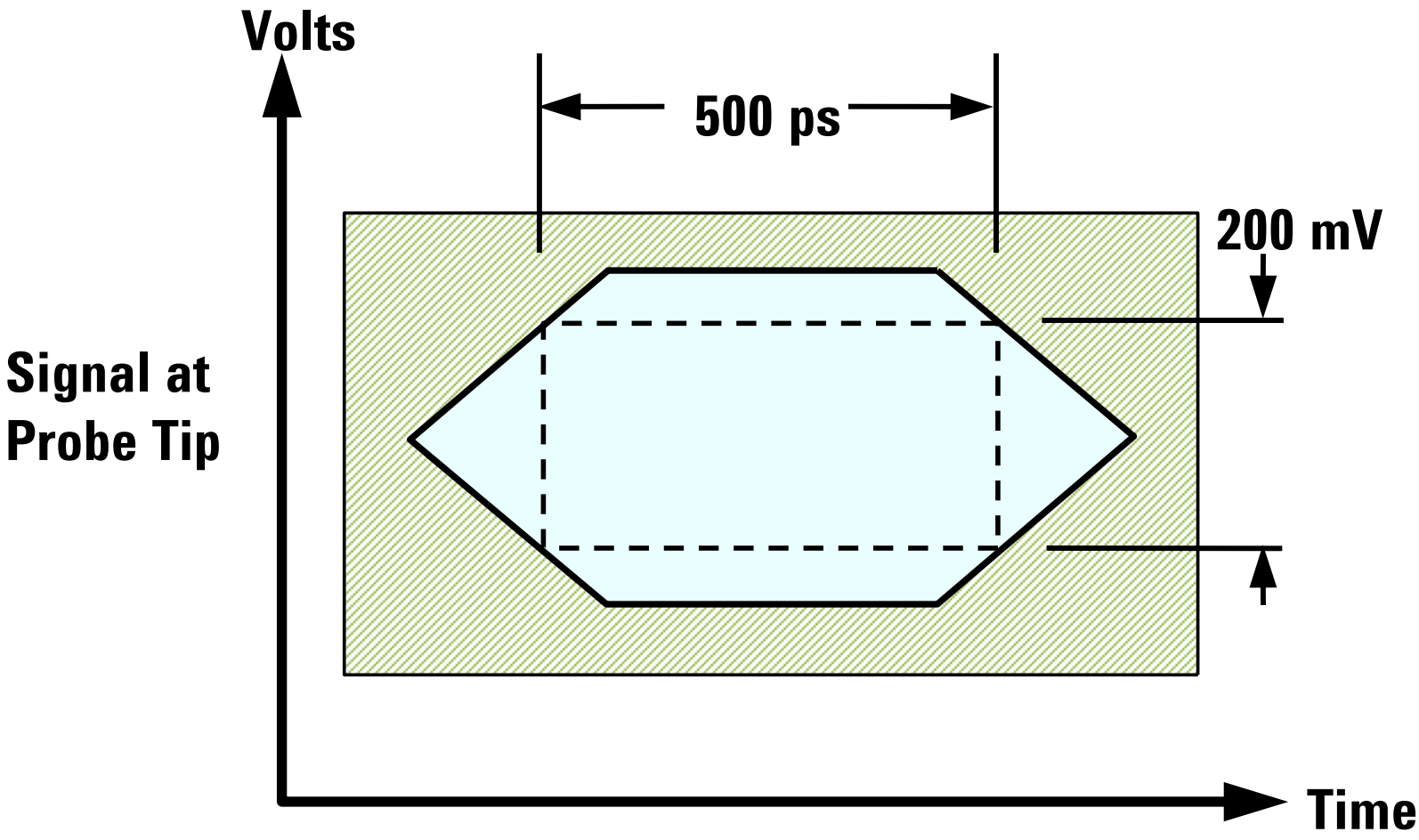
Required Eye Opening at Probe Tip - 16760 (LVDS)



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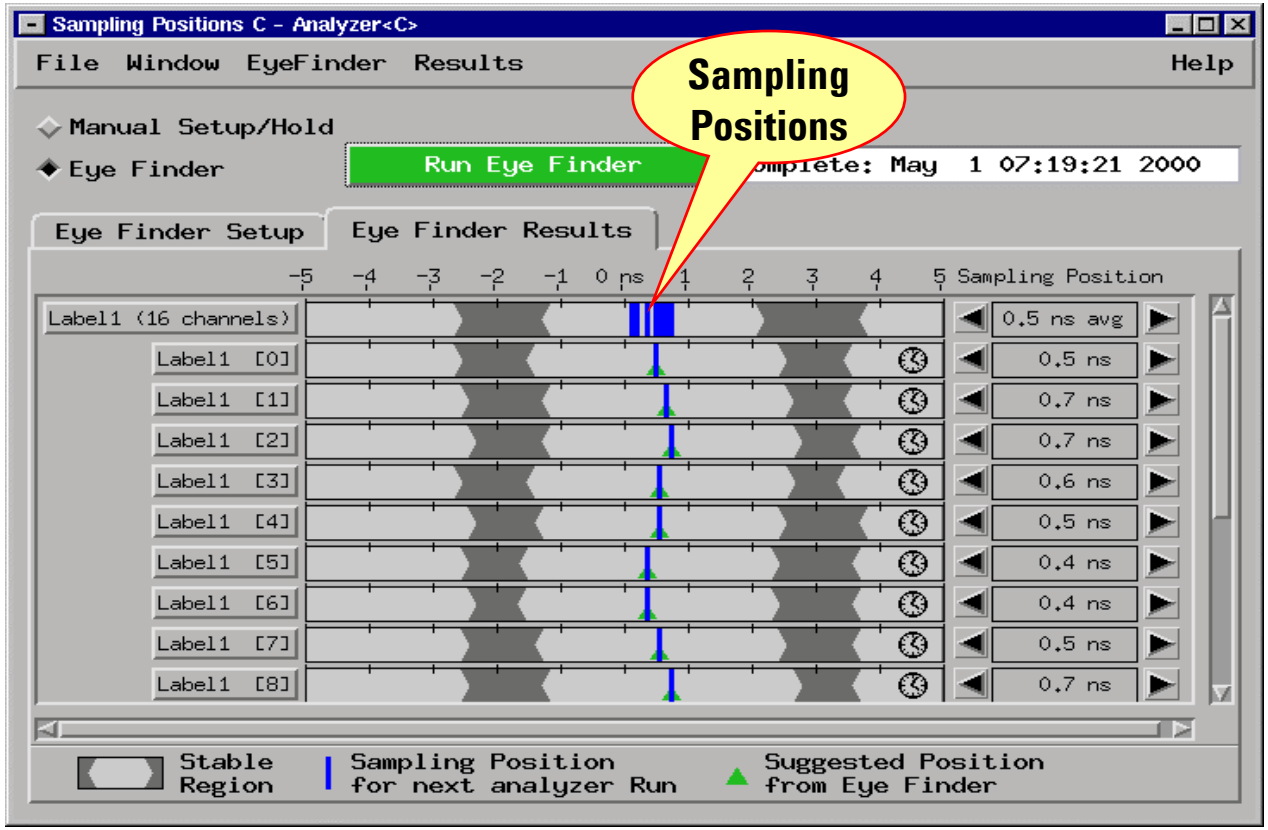
Common Problems in Router Subsystem Turn-on

- **Data Corruption**
  Analyze channel-to-channel Skew, signal integrity
- **Bus Lockup/Inactivity**
  Detect Bus inactivity
- **Throughput & Latency**
  Measure Packet Throughput
  Measure Packet Latency Between PHY and DDR
  Measure PHY Transmit/Receive Latency
- **System Overload**
  Find Cause of Dropped Packets
- **Incorrect Packet Forwarding**
  External Trigger Arming Examples

Analyze Channel-to-Channel Skew



- Eye Finder automatically adjusts setup/hold window position
- Interactive display allows for manual override

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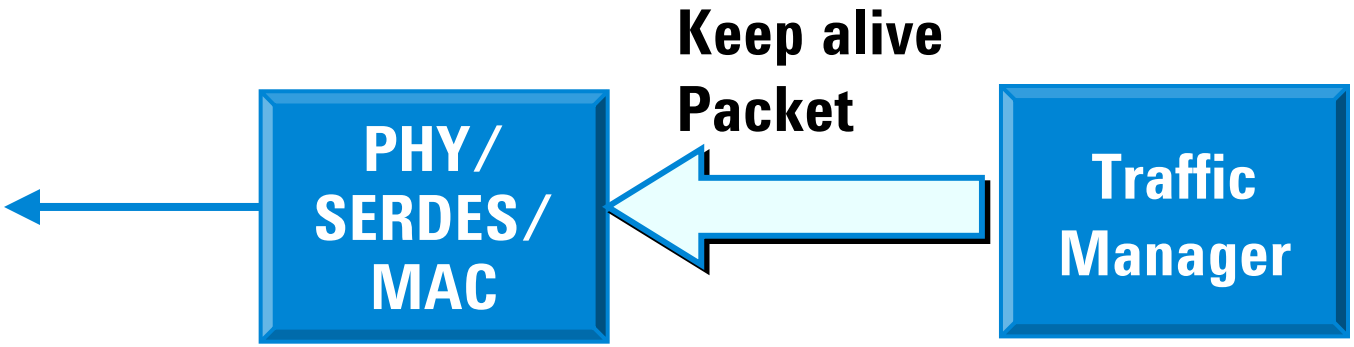
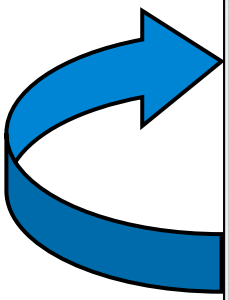
Detect Bus Inactivity

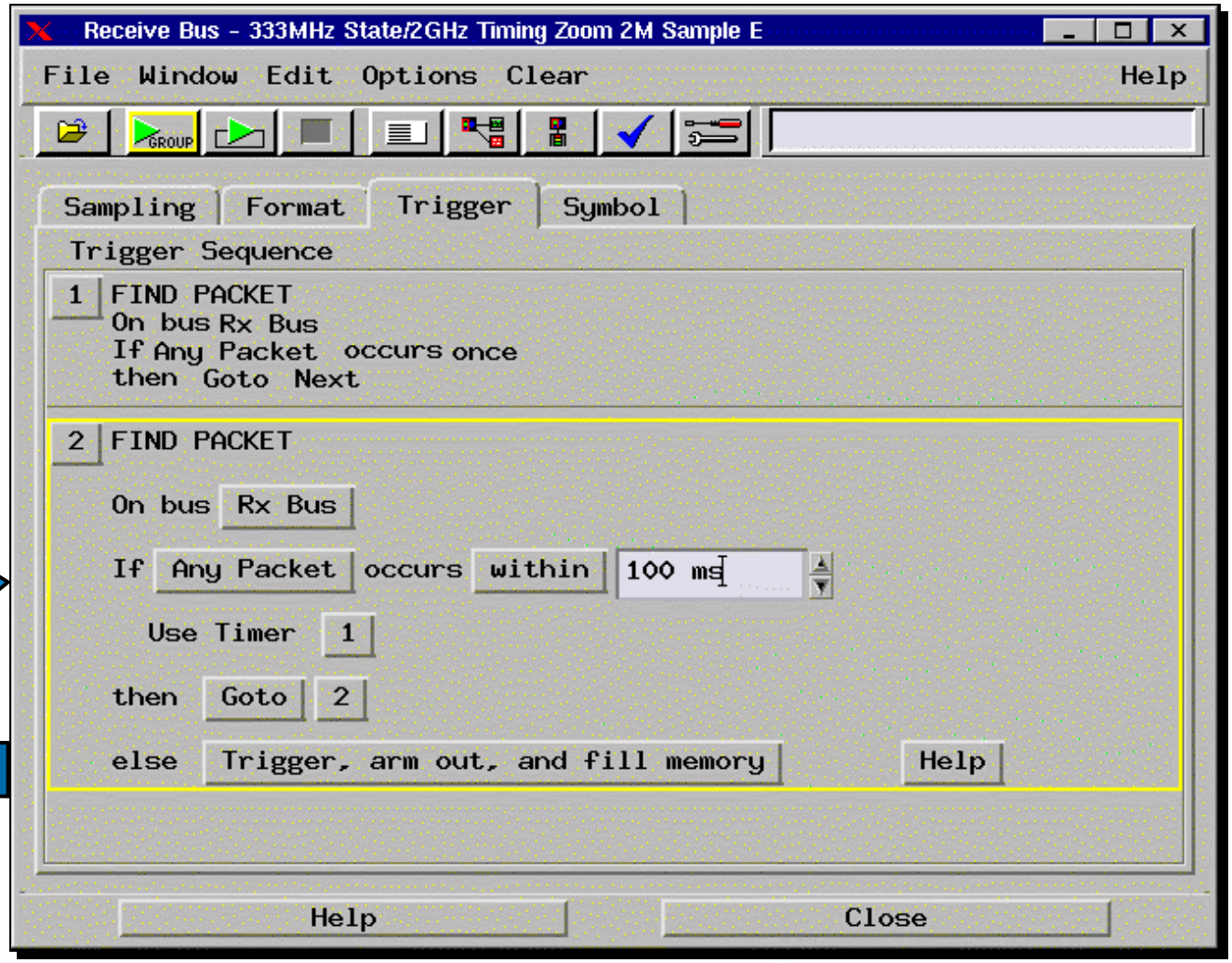


- Healthy links transmit keep alives

Detect Bus Inactivity – Trigger Setup

Loop as long as packets occur every 100 msec





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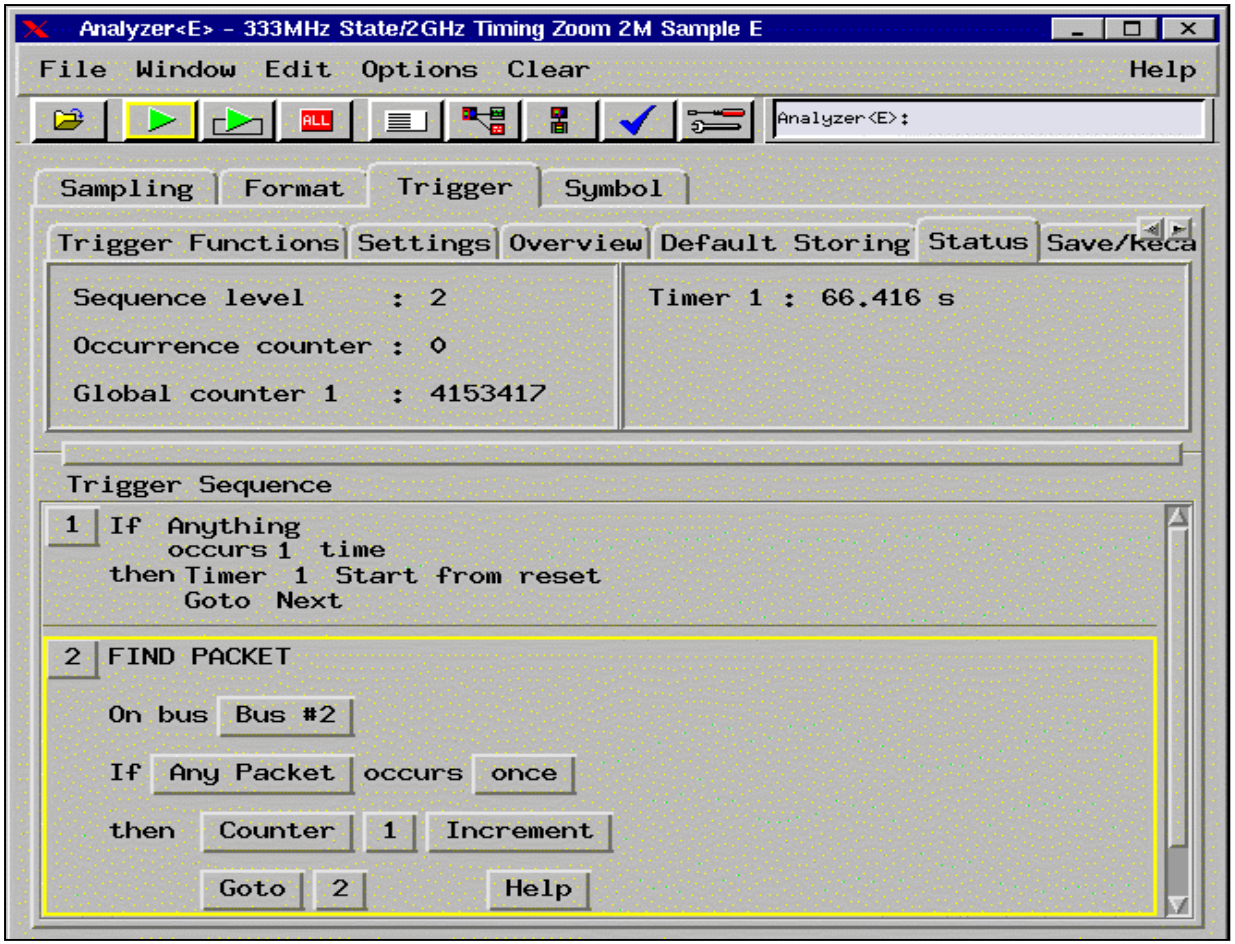
Measure Packet Throughput



- **Packets/second = 4153417/66.416**

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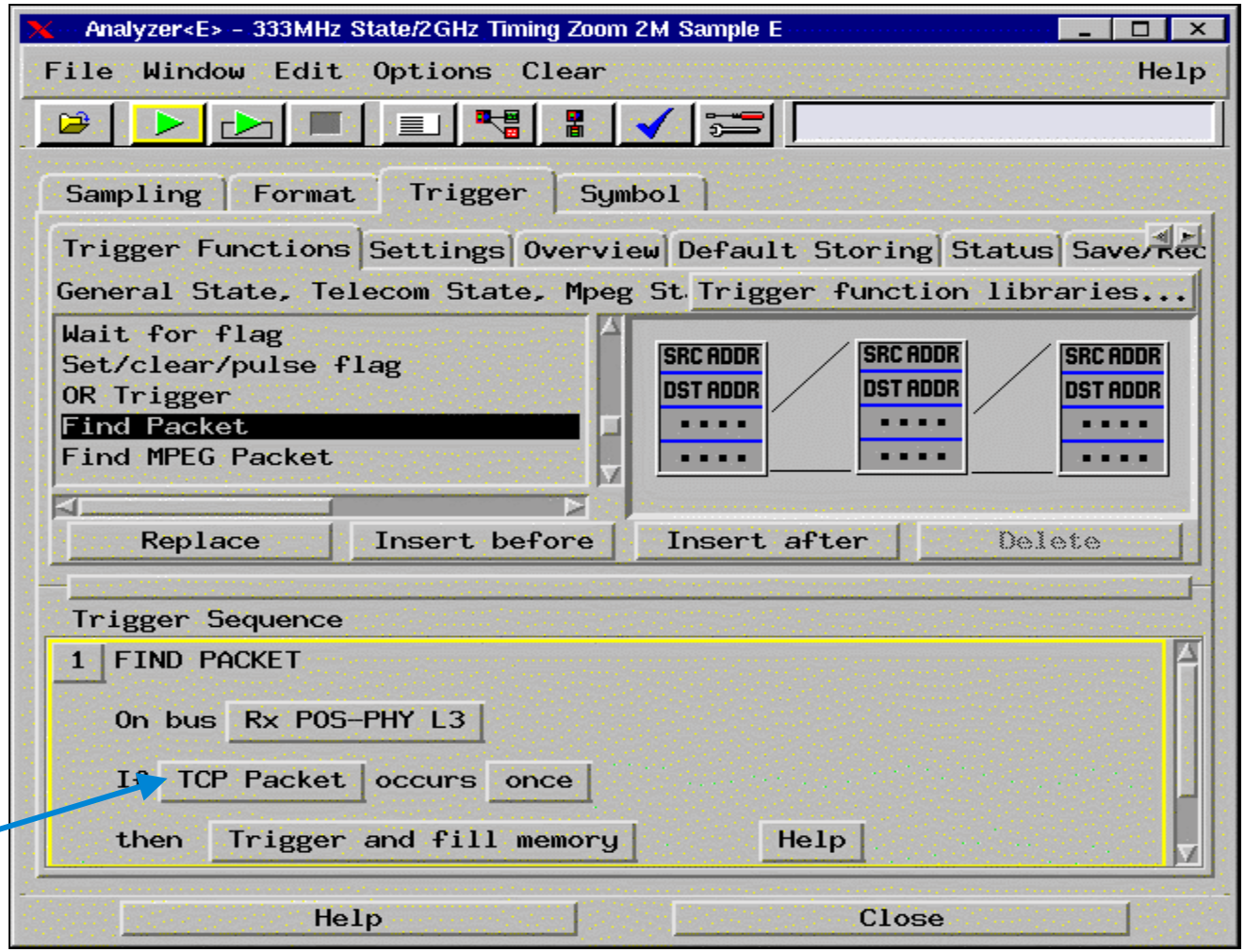
Trigger on Specific Header Fields



Event

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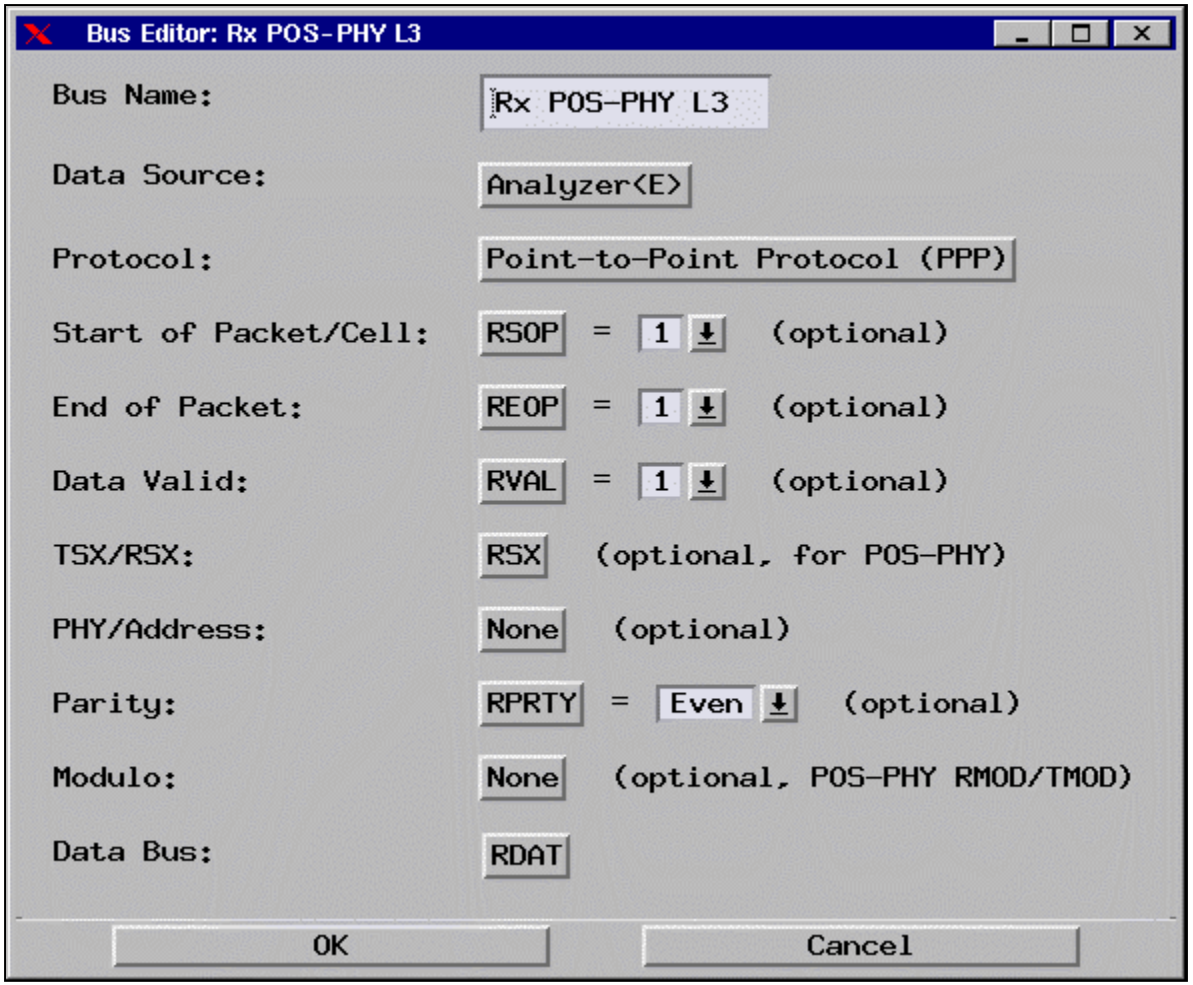
Packet Trigger Bus Editor



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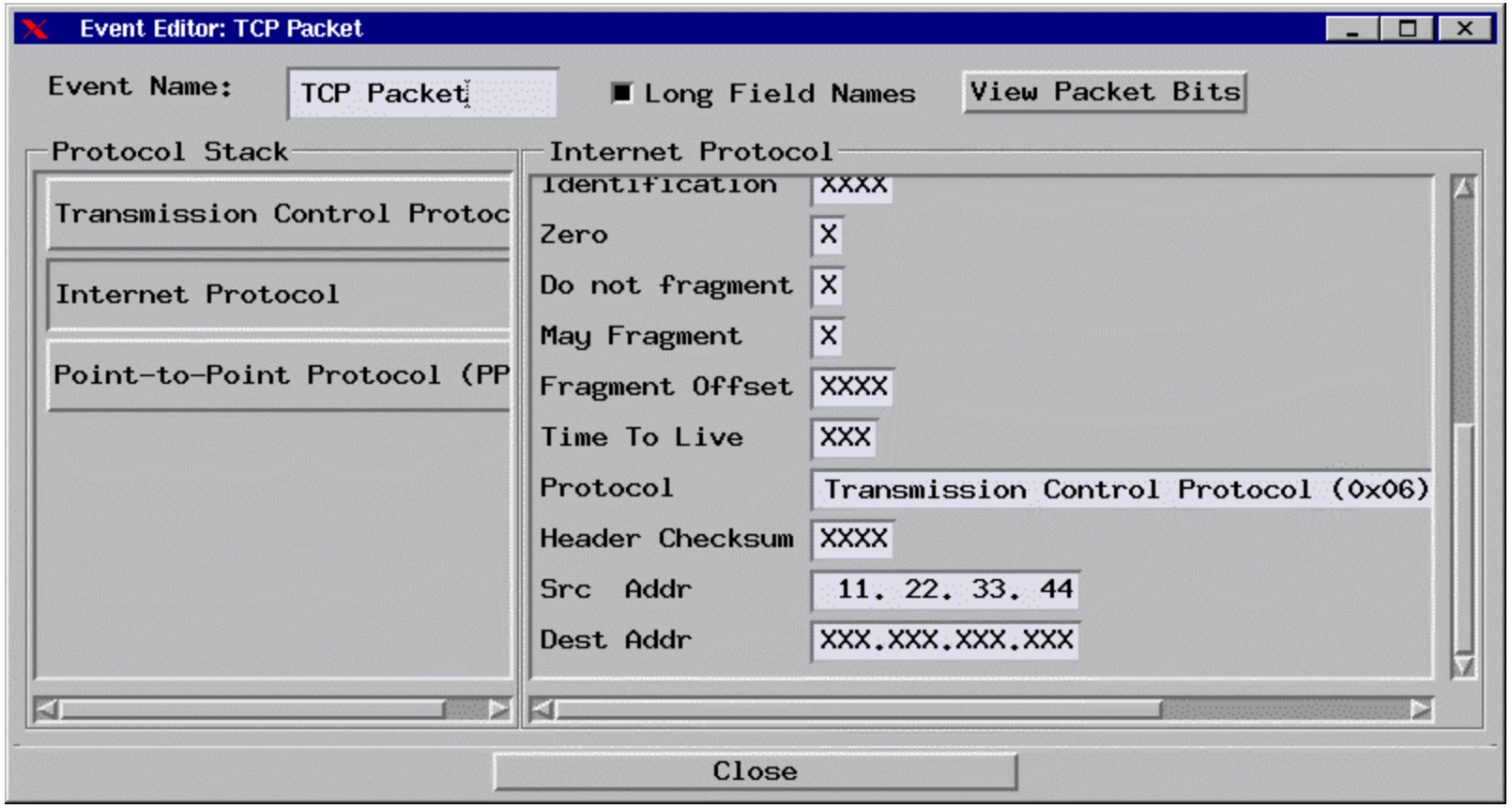
Packet Trigger Event Editor



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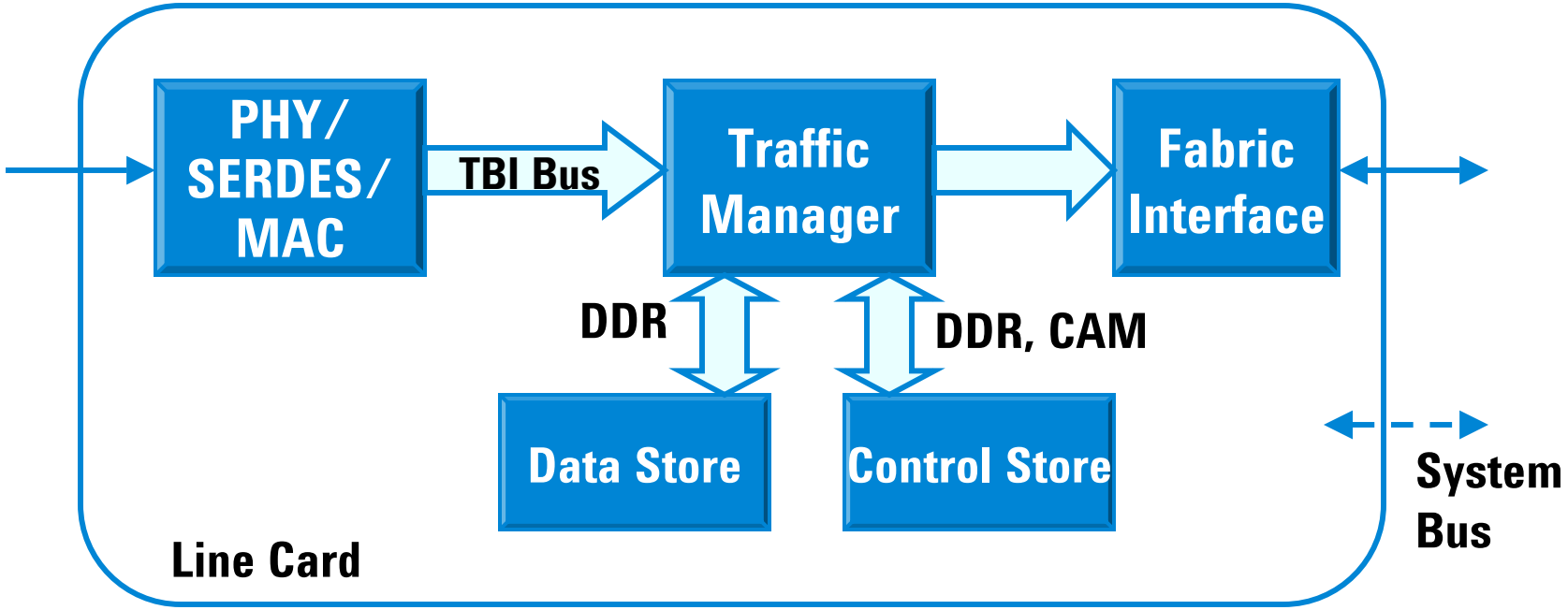
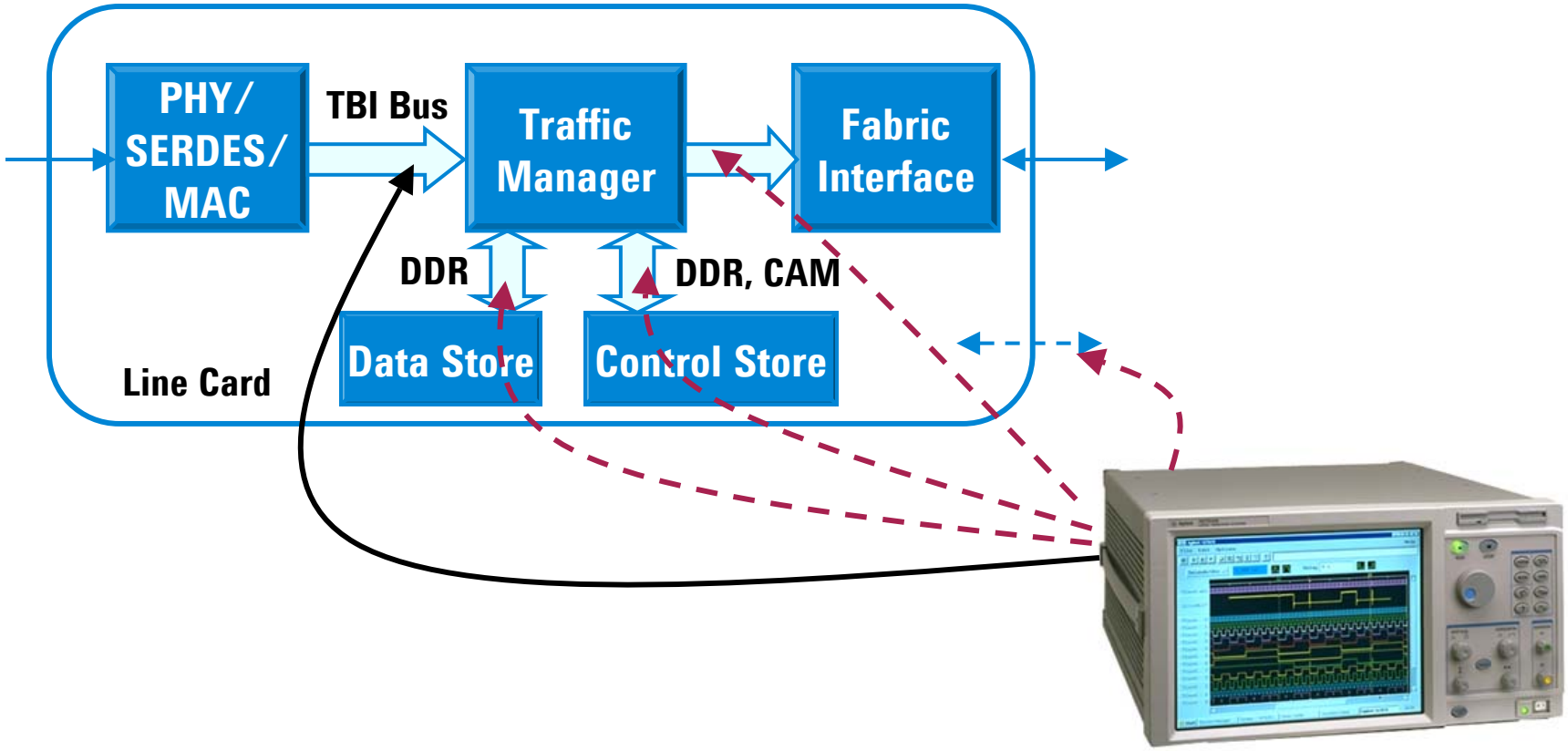
Measure Latency Between PHY & DDR



Possible causes:

1. Packets buffered in data store too long
2. Traffic manager takes too long to process
3. Route lookup goes off-board, and system board is slow to respond
4. Buffering issues causing port contention.

Packet Latency Between PHY & DDR



1. Trigger on Start of Packet
2. Use Intermodule trigger to correlate data store activity

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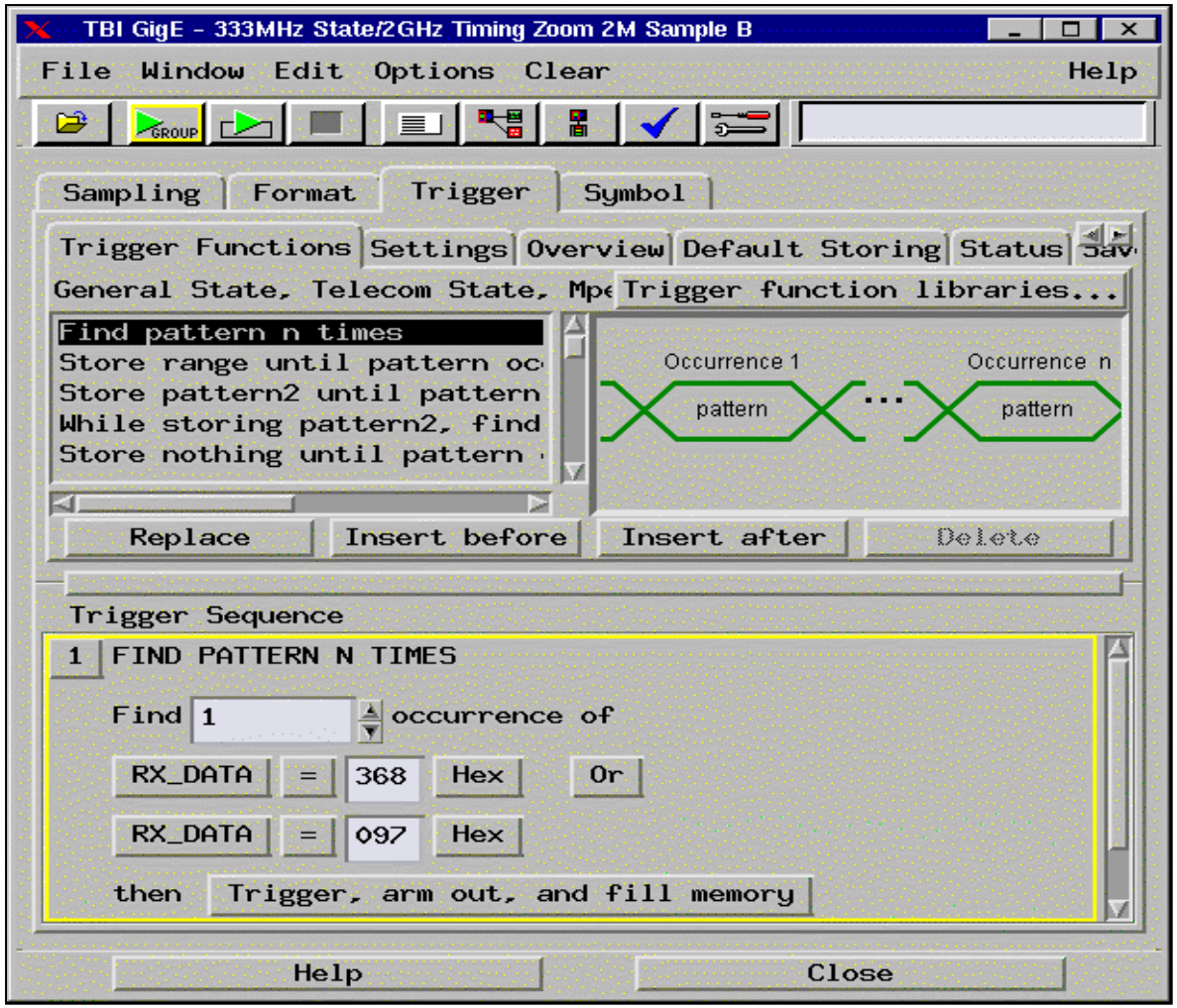
TBI Bus Trigger



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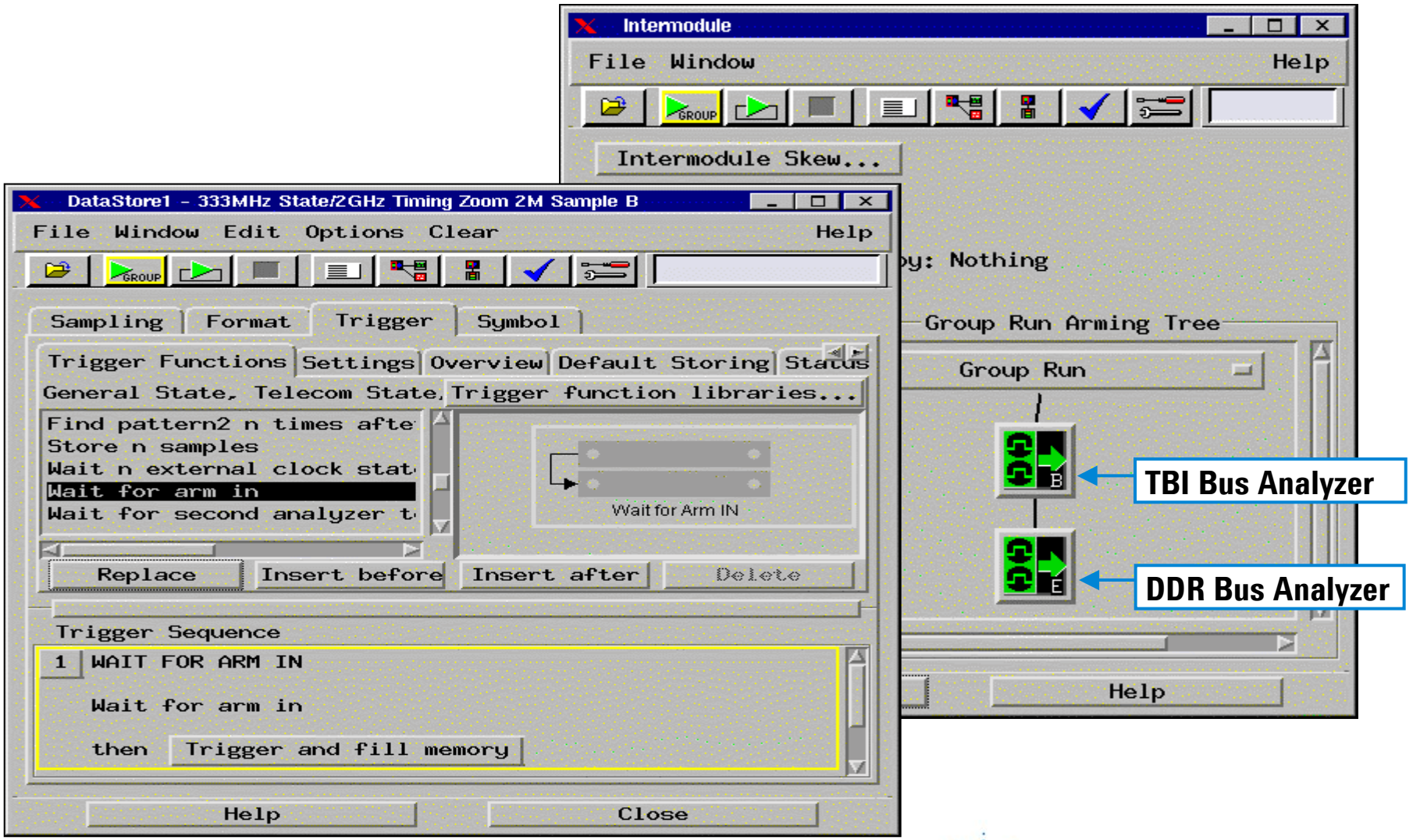
Data Store Bus Trigger



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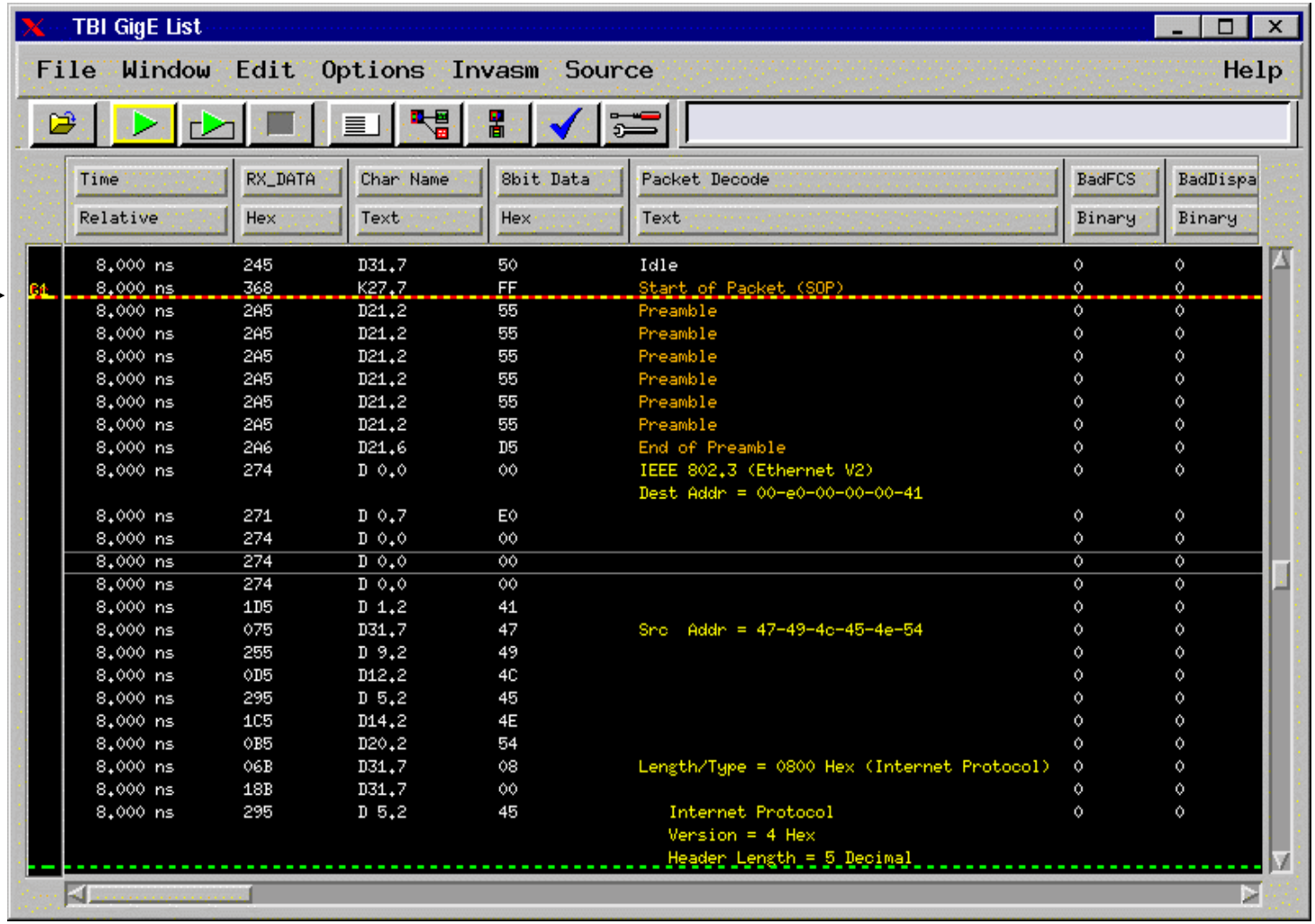
TBI Bus Decode Listing

Start of Packet →



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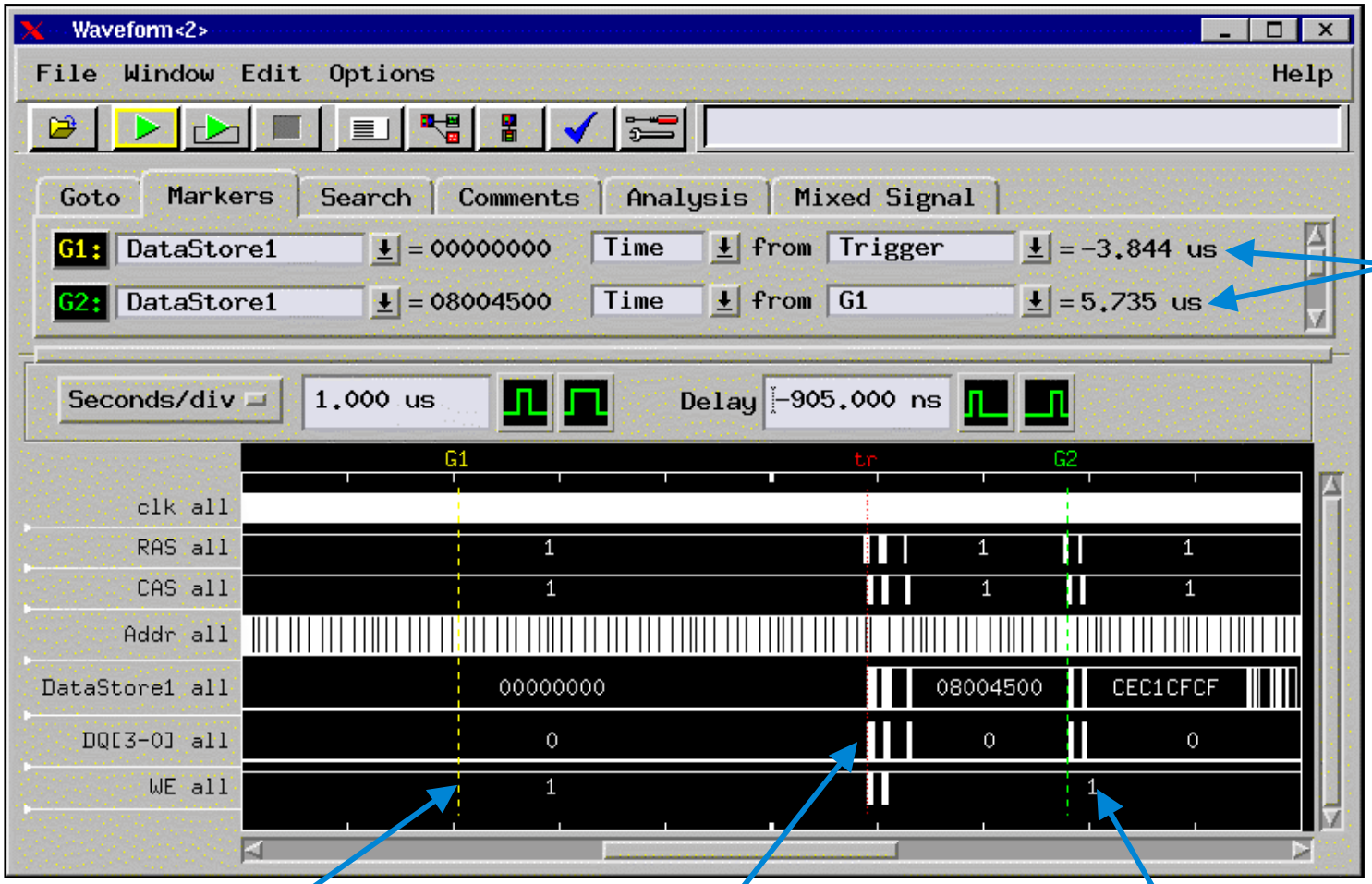
DDR Data Store Timing Waveform



Easy marker measure-ments

Packet arrives on Receive TBI Bus

Packet written to data store 3.8 usec later

Packet read back out of Data Store

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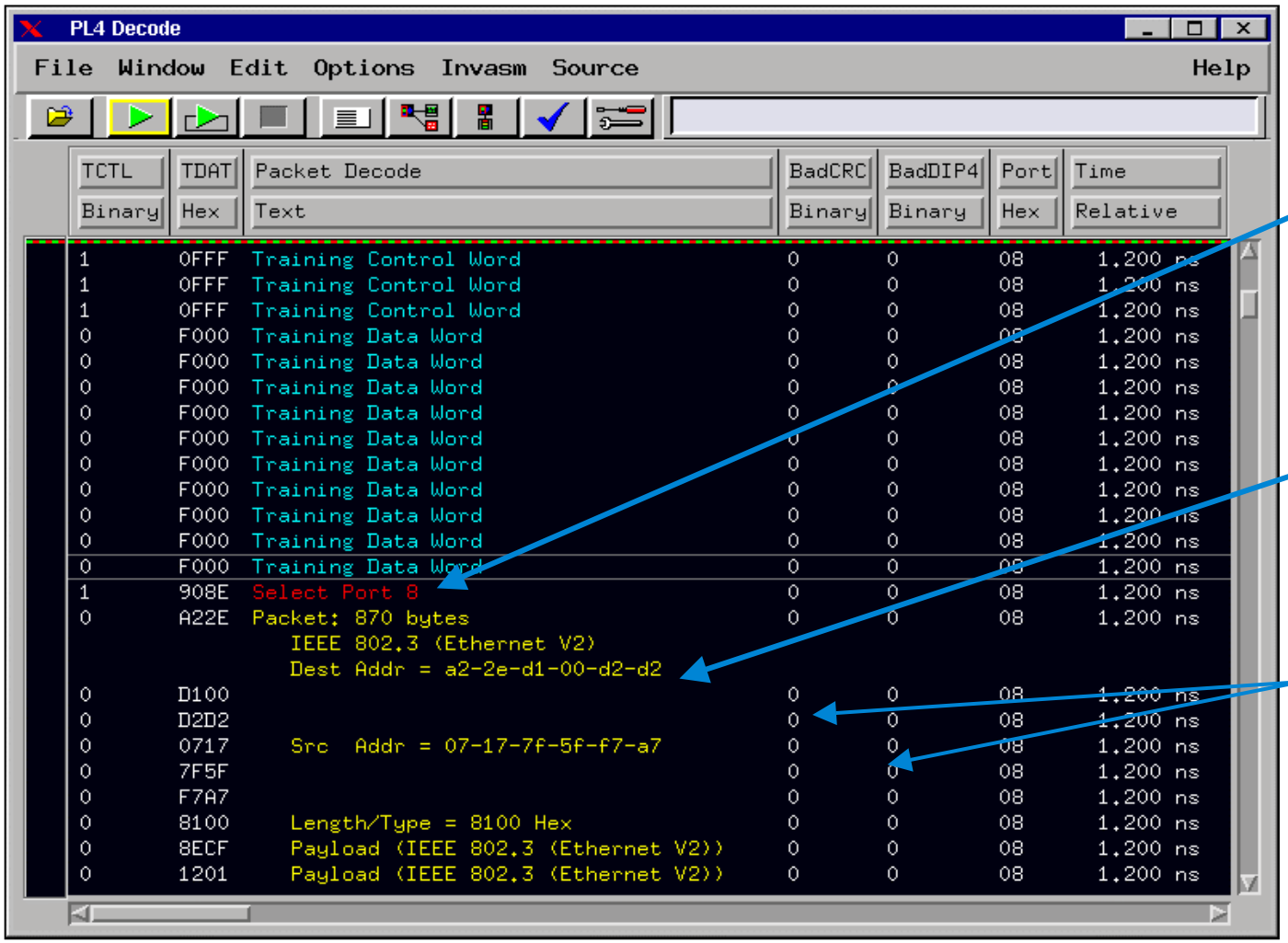
POS-PHY Level 4 Analysis



Reassemble packets from multi-port operation

Decode the PPP and TCP/IP stacks

Check DIP-4 Parity and CRC Codes

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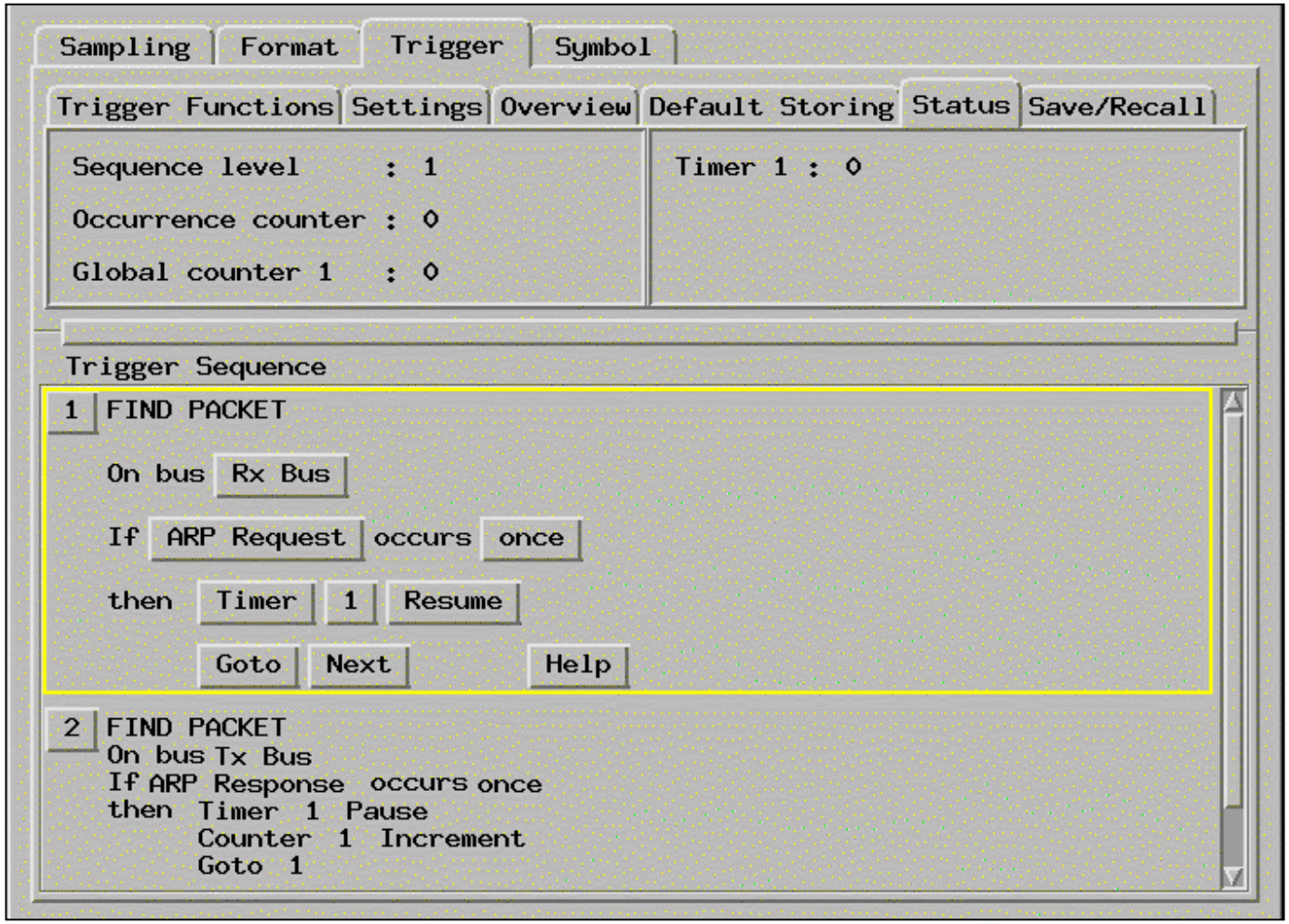
PHY Transmit/Receive Latency



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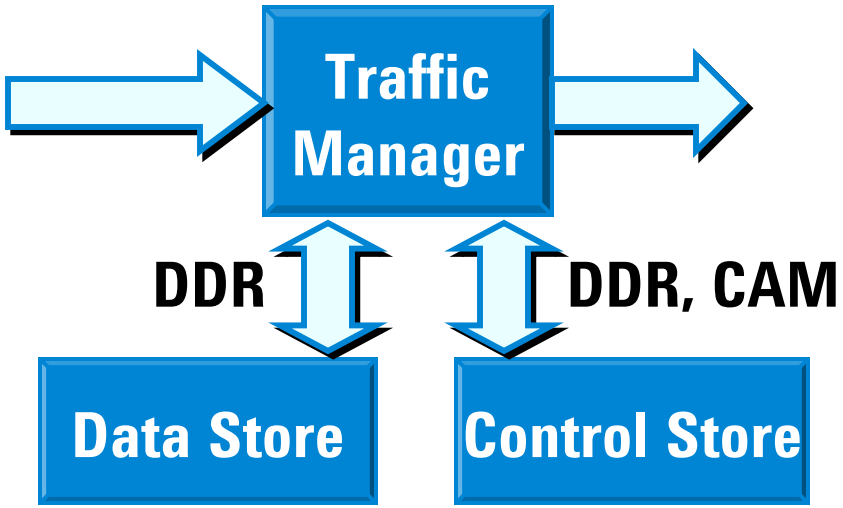
Find Cause of Dropped Packets



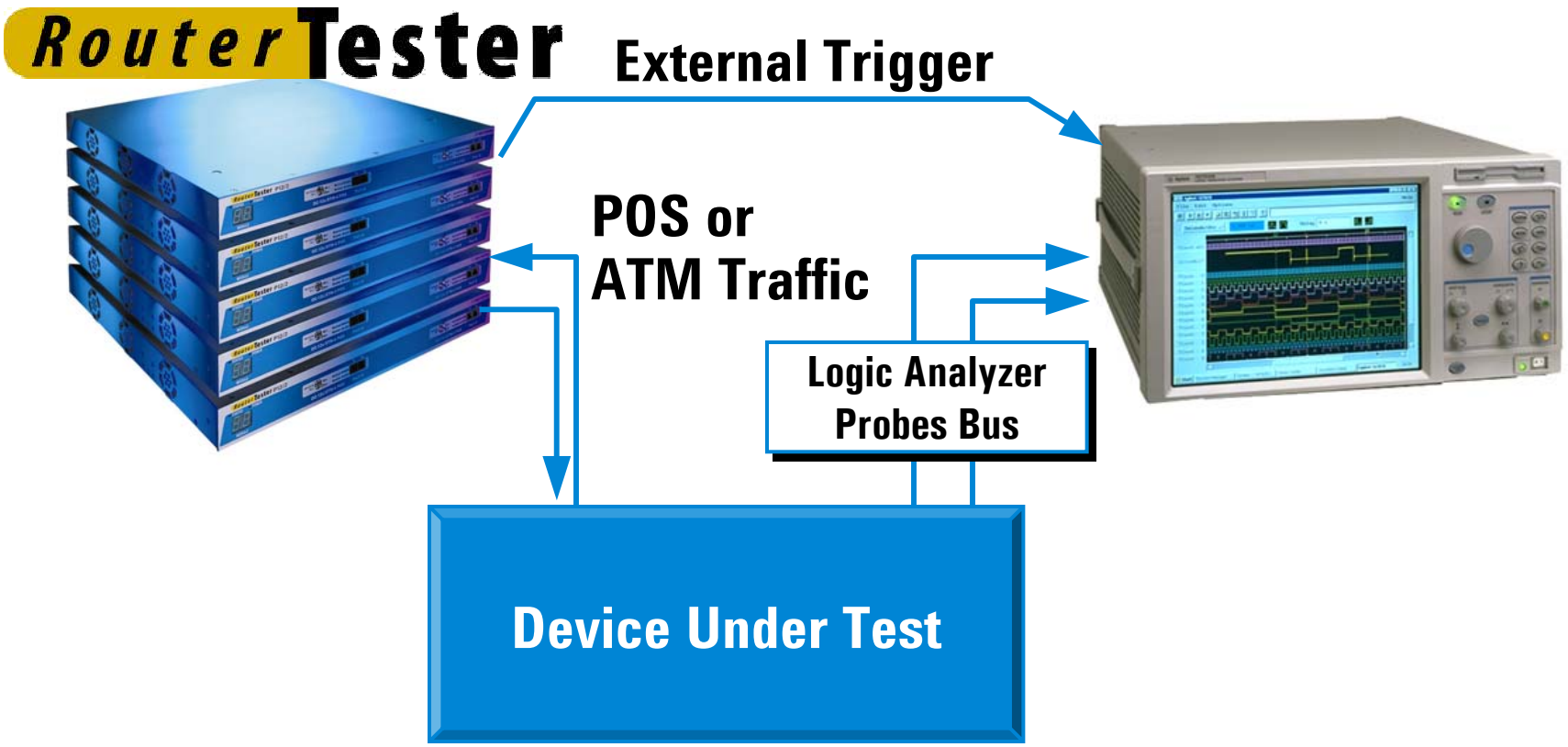
Possible Trigger Schemes:

- Address out of range in data store
- Signals indicating queue getting full
- Debug port on network processor

Possible causes:

- Latencies in route lookups
- Too much high-priority traffic
- Too many short packets
- Firmware/logic bugs in scheduling

Strategy - External Trigger Sources



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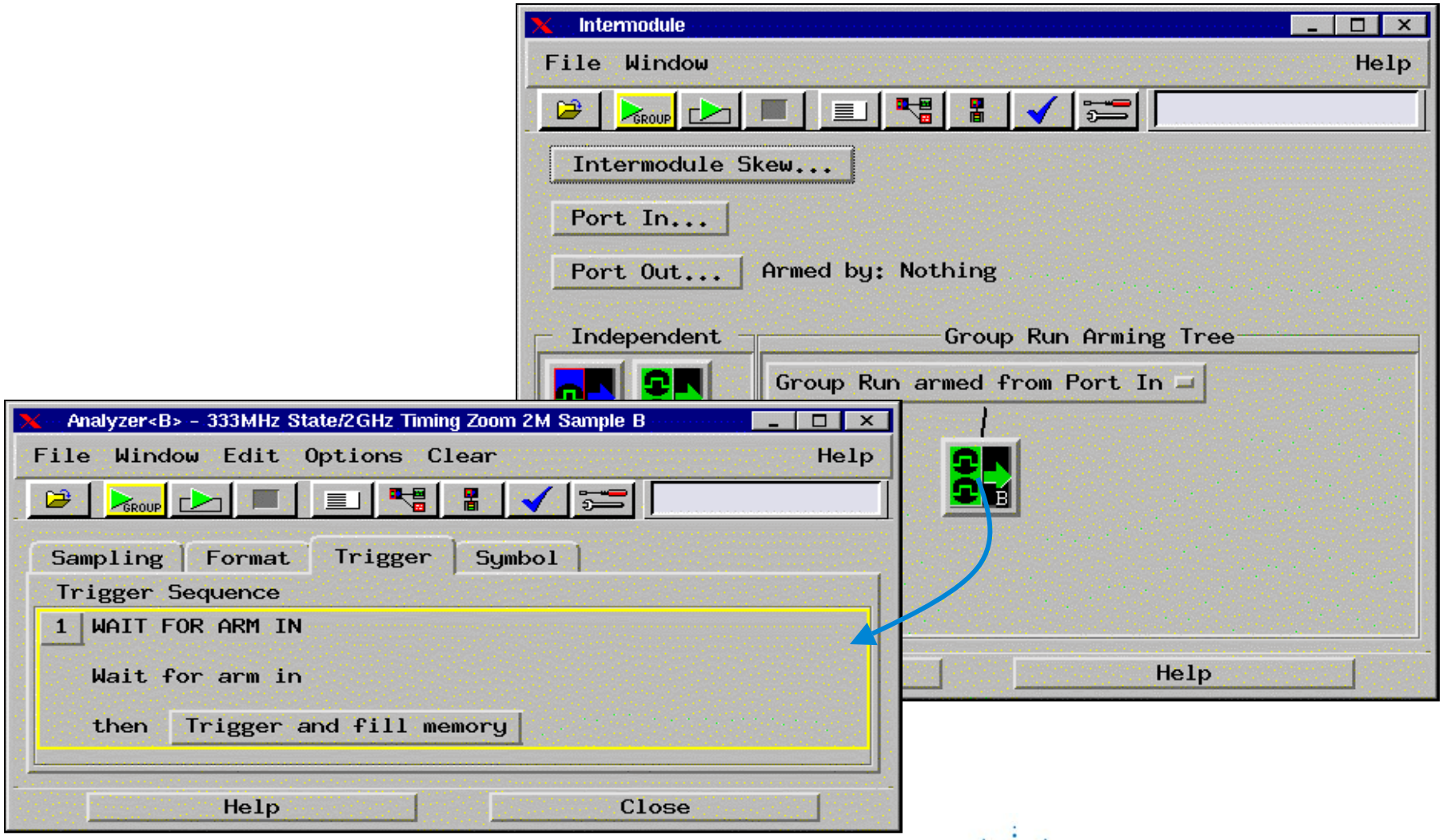
External Trigger – Analyzer Setup



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Protocol Decoding and Triggering

Bus	Protocol(s)	Packet Trigger	Decode Software	Product
UTOPIA L1-3	ATM, Cells and AAL5	Yes	Yes	B4640B
POS-PHY-L3	POS, Ethernet	Yes	Yes	B4640B
POS-PHY L4 (SPI-4 Phase 2)	OC-192 POS, 10 G Ethernet	No	Yes	N4214A
MII, GMII	Ethernet, other non-segmented	Yes	Yes	B4640B
TBI (Gbit Ethernet)	Ethernet, or other non-segmented	No (8B/10B encoded)	Yes	N4212A
InfiniBand	SERDES 10-bit interface or cable	Yes (via N4207A analysis probe)	Yes	N4206A N4207A

Capture-only Buses

HyperTransport (LDT)	16760 (Solution coming from FuturePlus)
Rapid/IO	16760 (Decode tool coming soon)
CSIX	1675X

Note - Packet trigger macro not available on 16760 in high-speed LVDS mode

Conclusion

- Troubleshooting bleeding-edge systems is critical
- Systems must be designed for testability
- Logic analysis tools are essential for router debug
  - Probe LVDS signals
  - Trigger on packets
  - View decoded protocols

For more information see the R&D Central Website:

http://www.agilent.com/find/randd

  - Discussion forums
  - Application notes