



Agilent Technologies

Debugging IP Router Subsystems-- Logic Analysis Tools for POS, Gigabit Ethernet and ATM

September 21, 2001

presented by:

Scott Ferguson

Agenda

- **Overview of router architecture & subsystems**
- **Designing in testability**
- **Example problems & solutions**
- **Conclusion and summary**

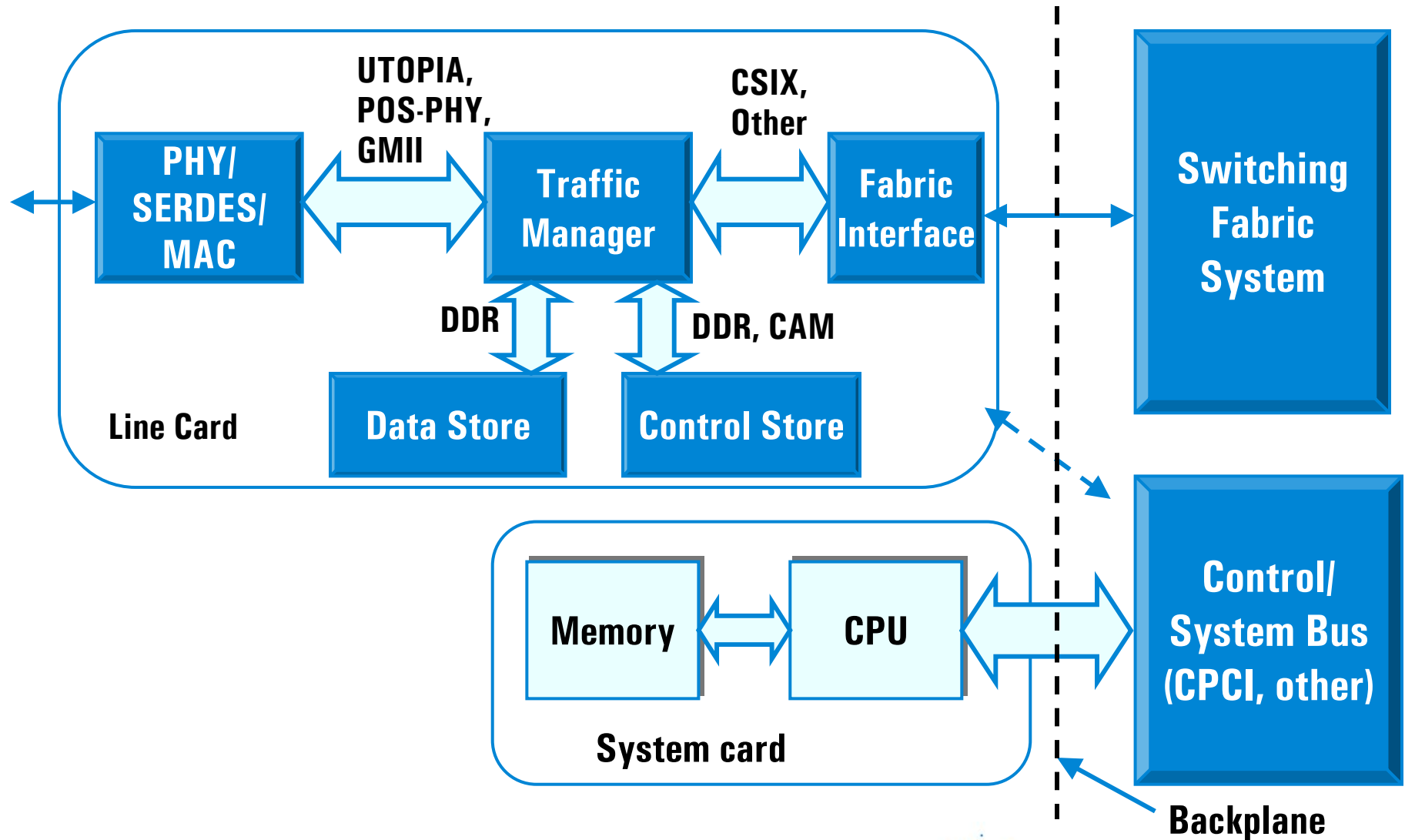


Bandwidth Demand Fuels Competition

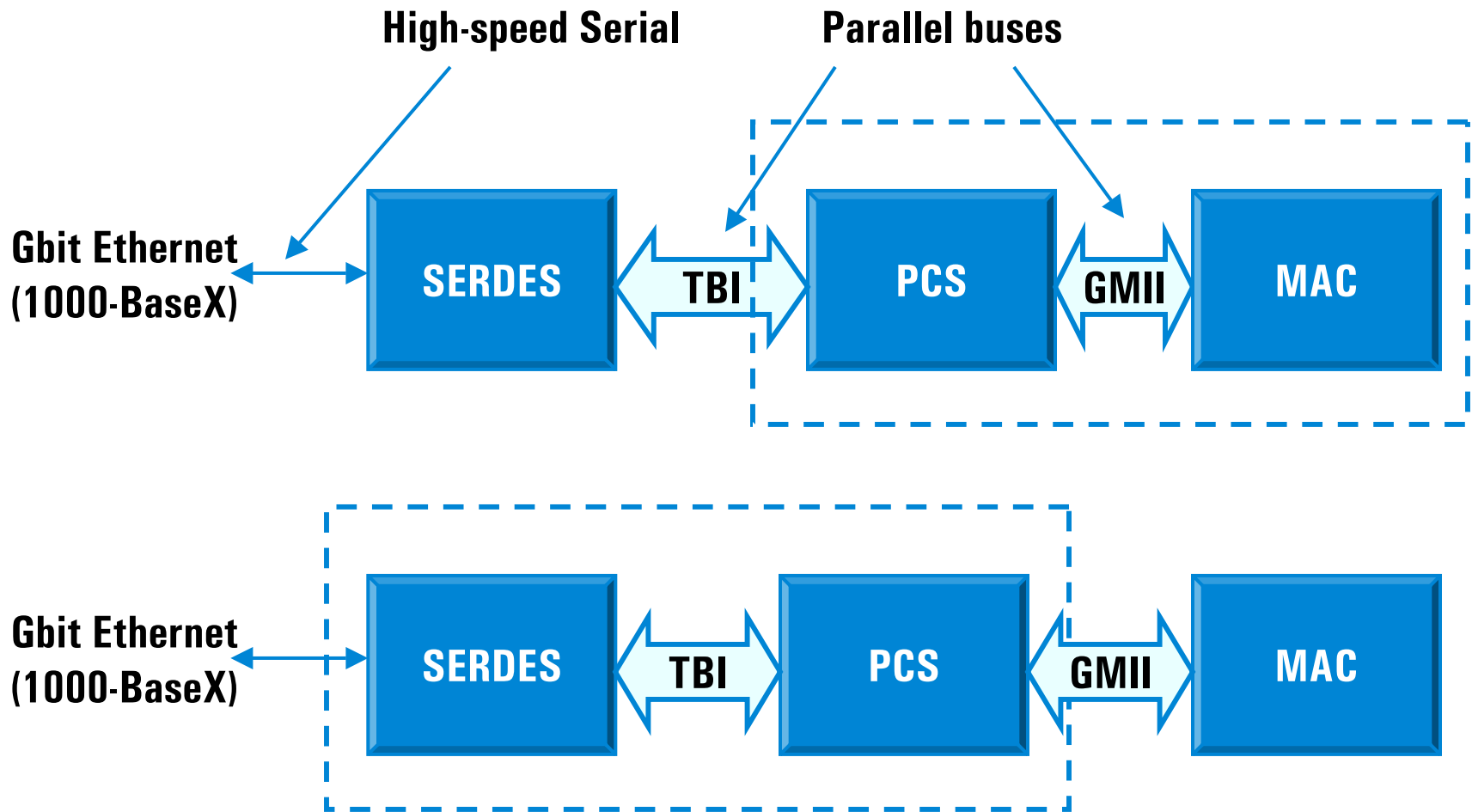
- **Highest (compliant) performance wins**
 - **Speed**
 - **Throughput**
 - **Intelligent response to dynamic environment**
- **Time to market is key**



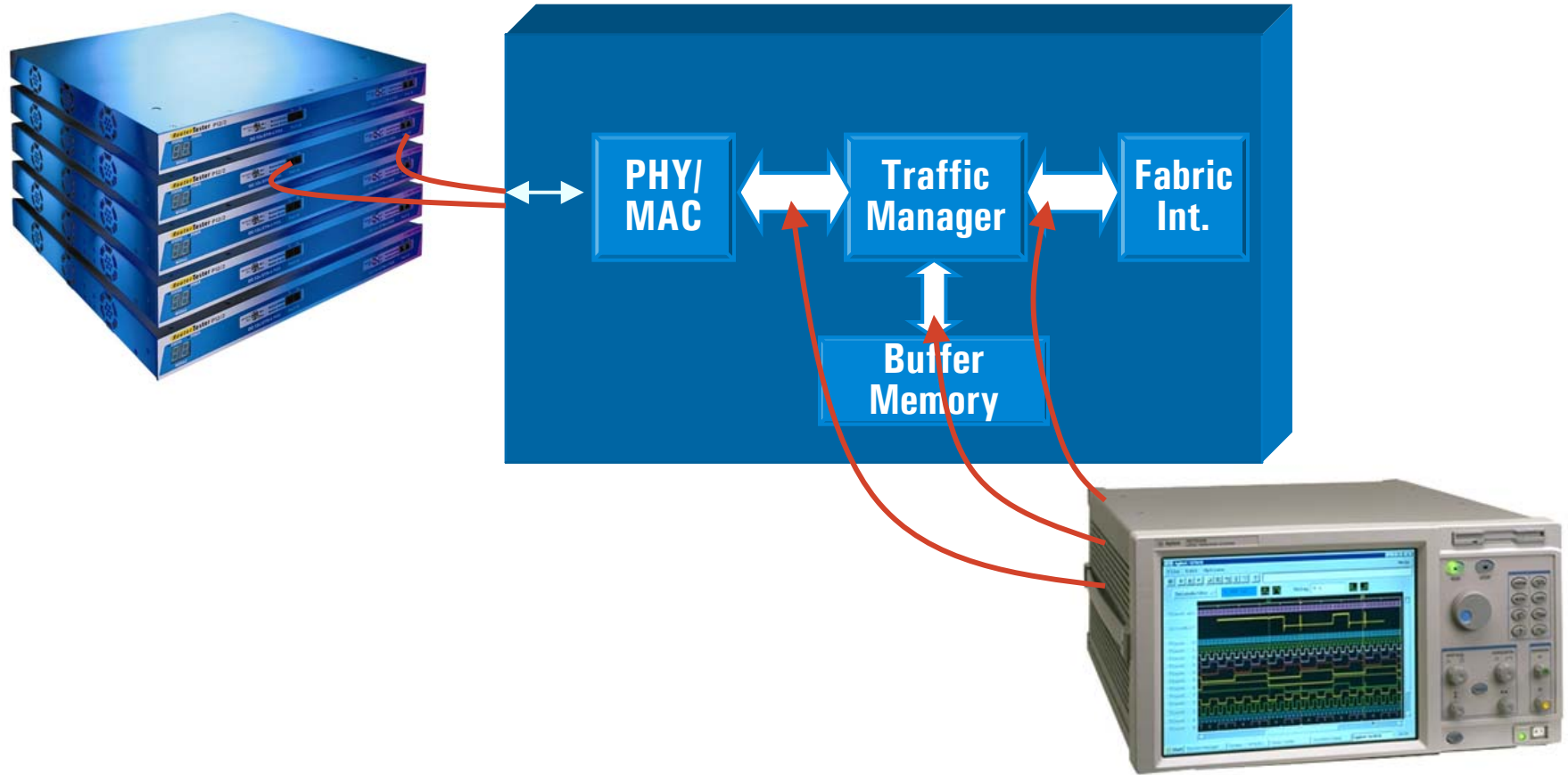
Sample Router Architecture



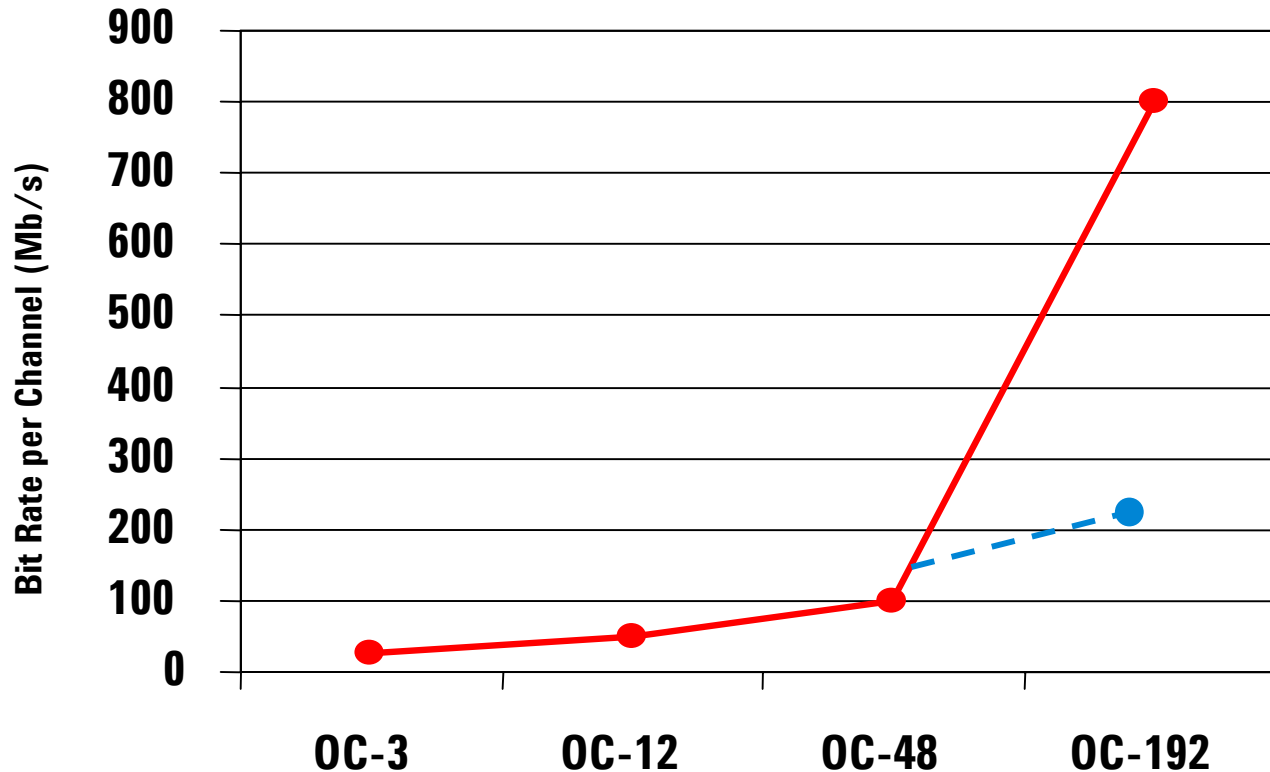
PHY Buses & Integration



Debugging Subsystems



LVDS Breaks the Rules

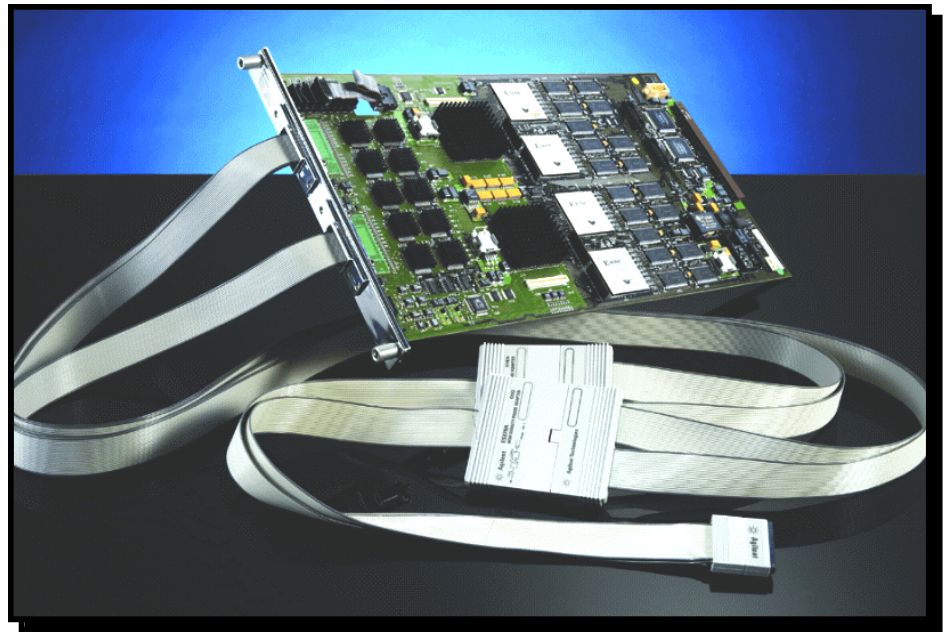


	OC-3	OC-12	OC-48	OC-192
Line Rate	155 Mb/s	622 Mb/s	2.5 Gb/s	10 Gb/s
Bus Width	8 bits	16 bits	32 bits	16 bits (diff. pairs)
Channel Bit Rate	25 MHz	50 MHz	100 MHz	800 Mb/s (400 MHz)



New Logic Analysis Tools

- **New 16760 state/timing module captures LVDS signals at up to 1.25 Gb/s (1.5 Gb/s coming soon)**
- **500ps setup/hold window**
- **10 ps setup/hold resolution**
- **Eye Finder technology automatically adjusts setup/hold window position**
- **64 M sample depth, 34 channels (260 Mbytes, or 2.6 M packets @ 100 bytes/packet)**
- **200 mV sensitivity**

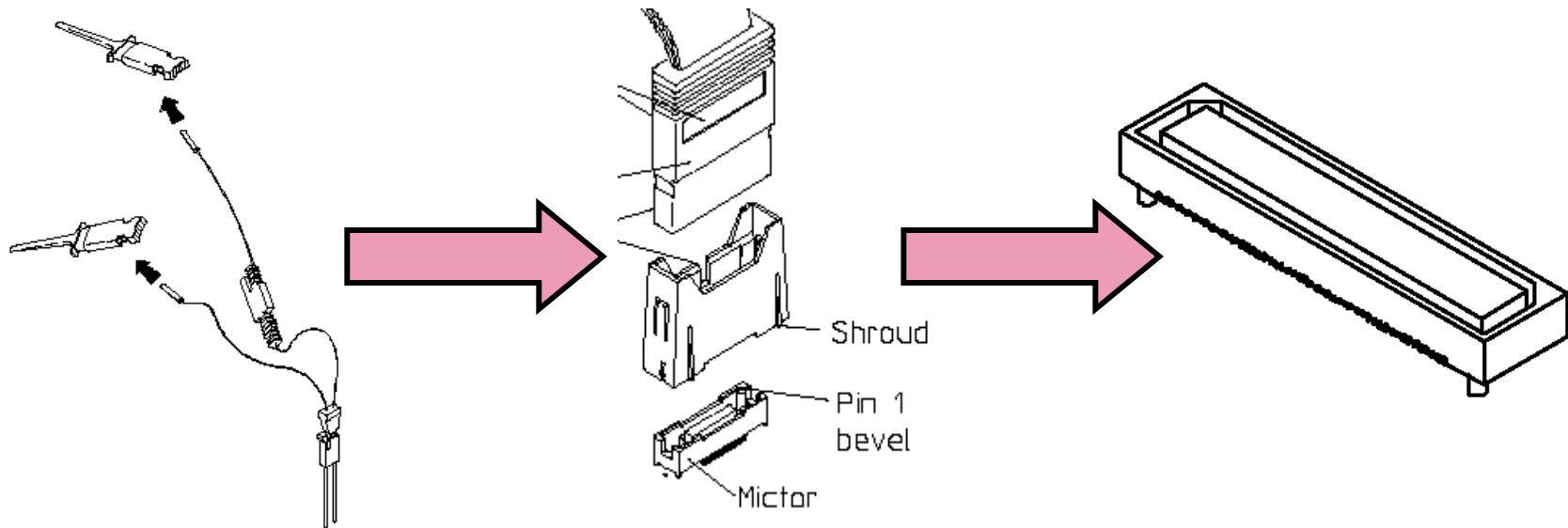


Designing in Testability

- **High speeds & LVDS create probing problems**
- **Probing must be considered before layout**
 - **Pay now, or pay later**
- **Probing changes circuit dynamics**



Designing in Testability

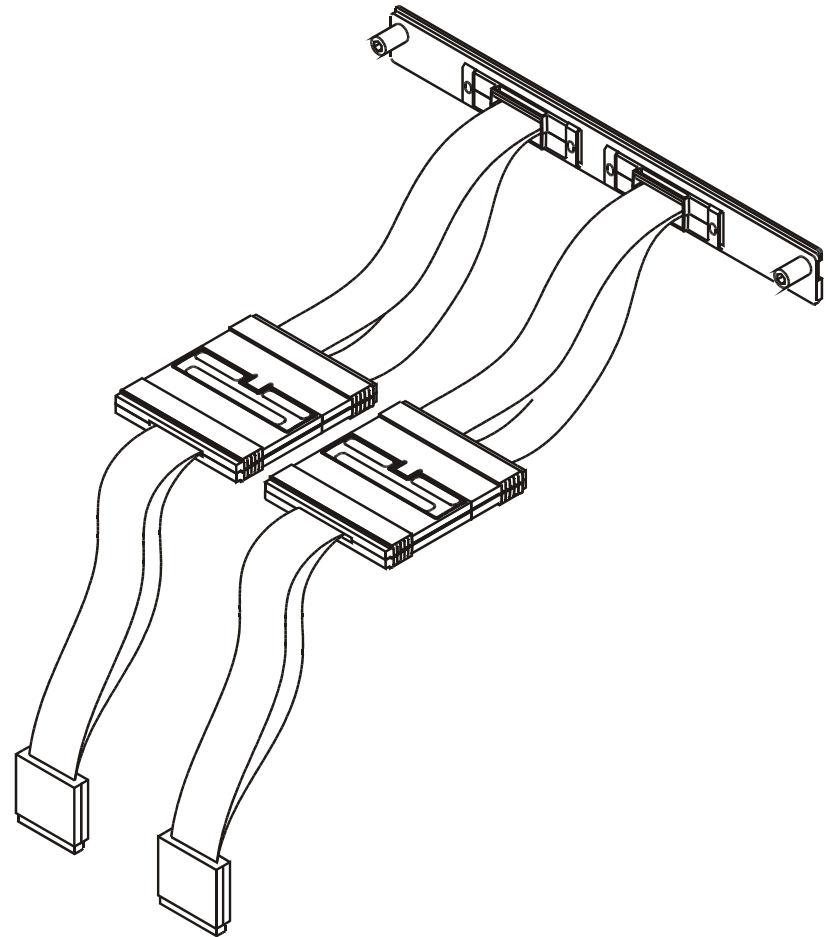


Year	Probing Method	Connection	Maximum Speed
1973-??	Flying Leads	Clip-on	300 MHz
1990's	AMP Mictor Connector	Surface mount	600 MHz
2001	Samtec BSH Connector	Surface mount	> 2 Gb/s



New Agilent Logic Analysis Probes

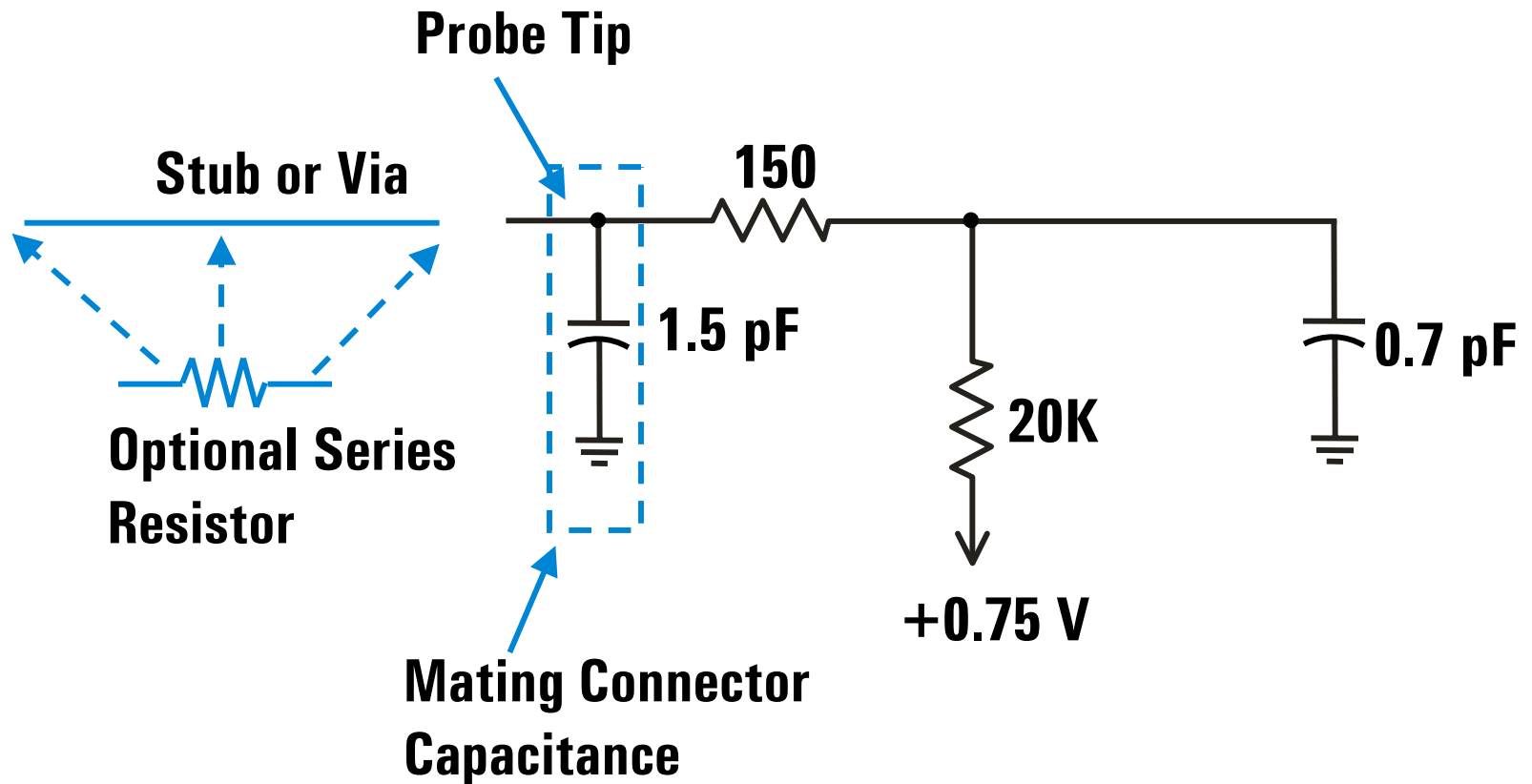
- **1.5 pF probing solution makes probing possible**
- **Differential probes have excellent channel-to-channel isolation at high speeds.**
- **Design probe connectors into target PC board**



www.agilent.com/find/probeguide



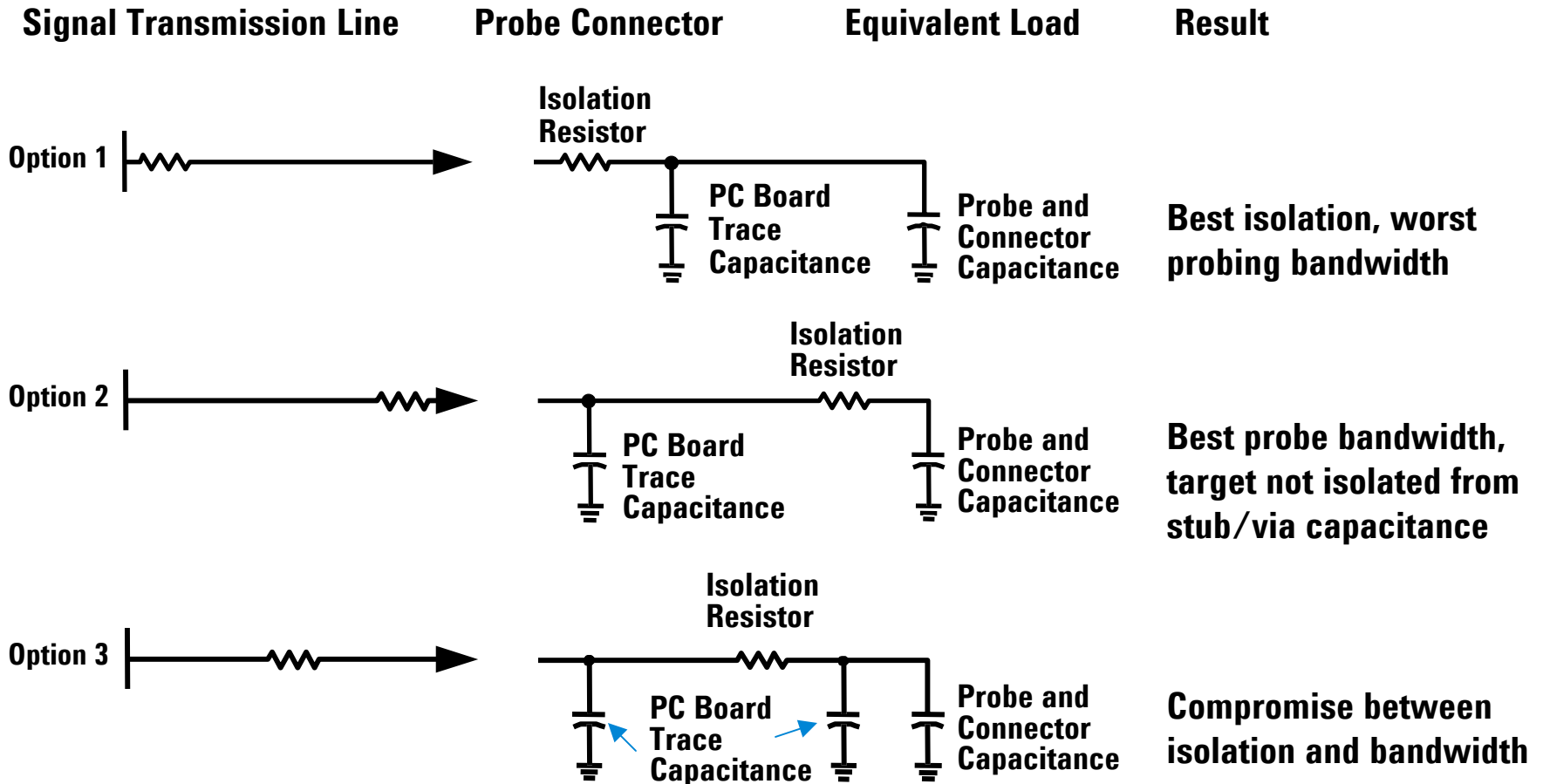
Probe Equivalent Load



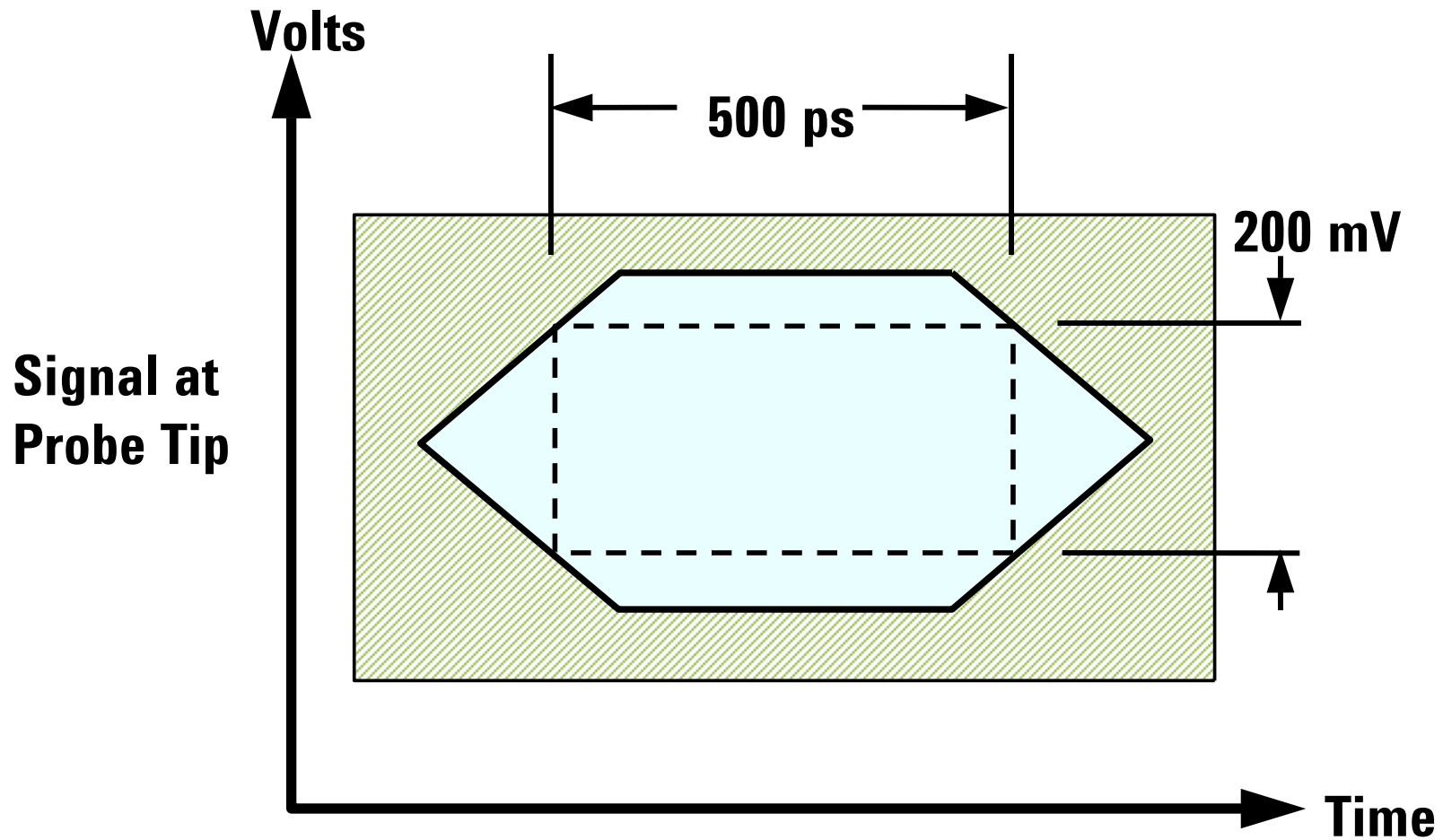
Signal Trace



Dealing with Stubs - Adding a Series Resistor



Required Eye Opening at Probe Tip - 16760 (LVDS)

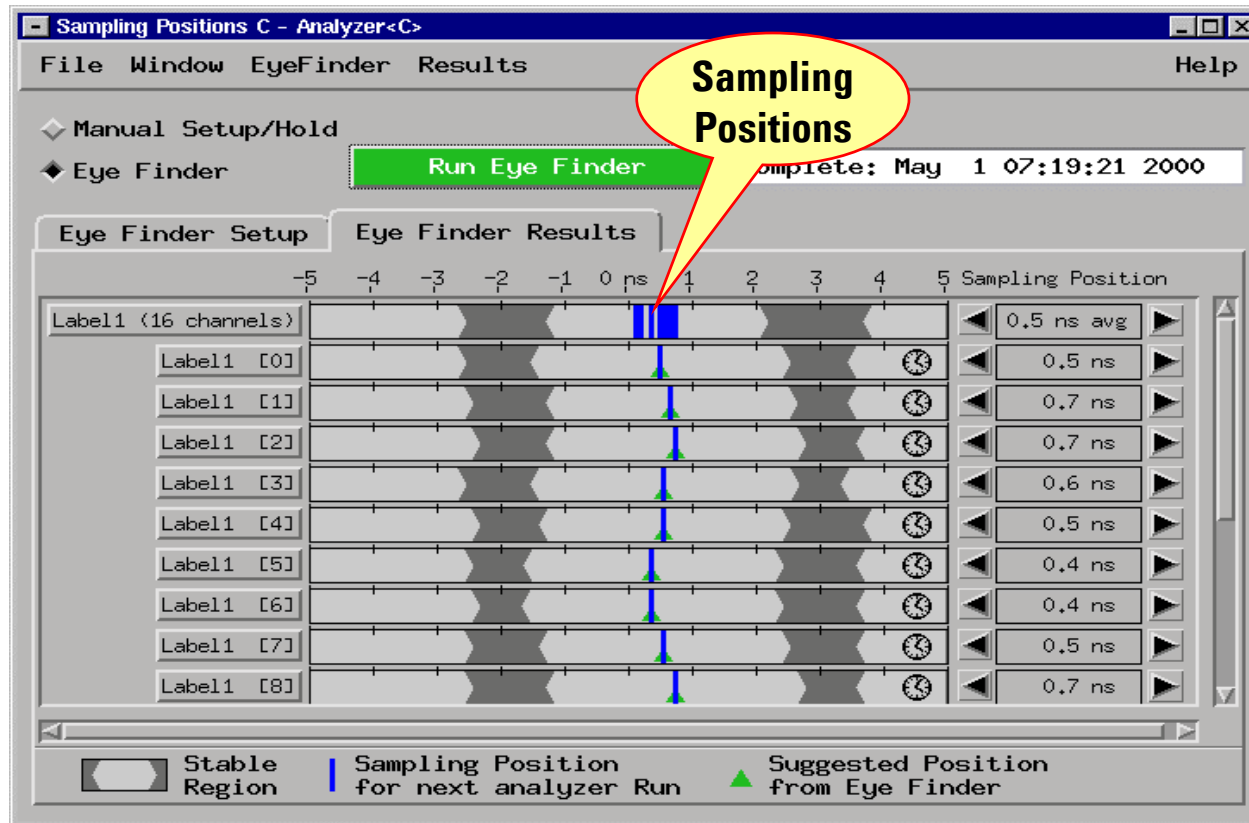


Common Problems in Router Subsystem Turn-on

- **Data Corruption**
Analyze channel-to-channel Skew, signal integrity
- **Bus Lockup/Inactivity**
Detect Bus inactivity
- **Throughput & Latency**
Measure Packet Throughput
Measure Packet Latency Between PHY and DDR
Measure PHY Transmit/Receive Latency
- **System Overload**
Find Cause of Dropped Packets
- **Incorrect Packet Forwarding**
External Trigger Arming Examples



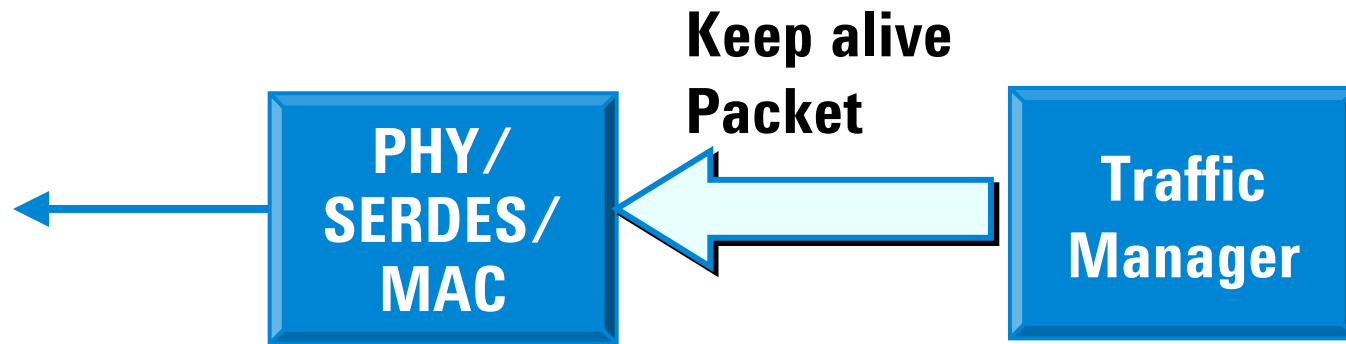
Analyze Channel-to-Channel Skew



- Eye Finder automatically adjusts setup/hold window position
- Interactive display allows for manual override



Detect Bus Inactivity

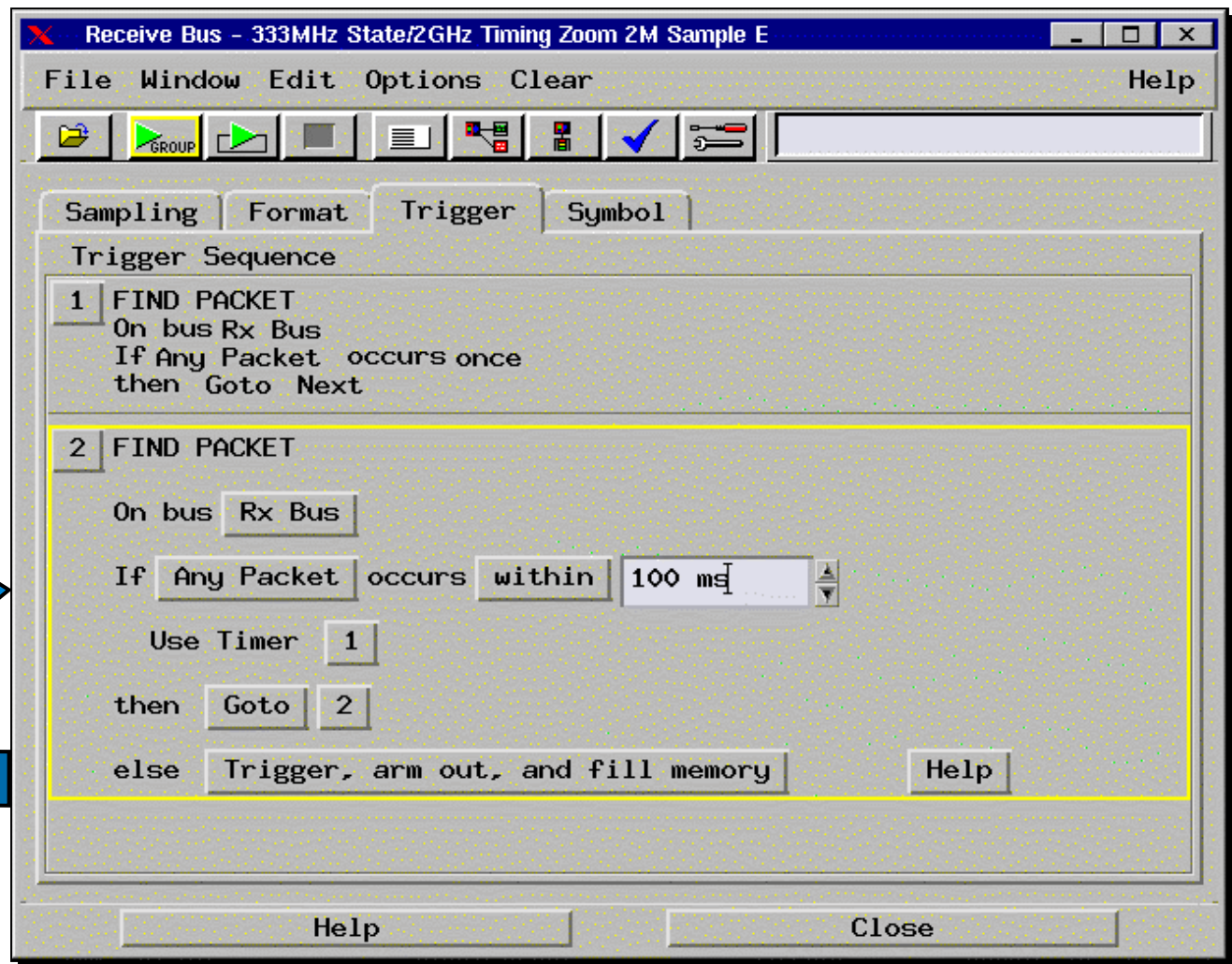
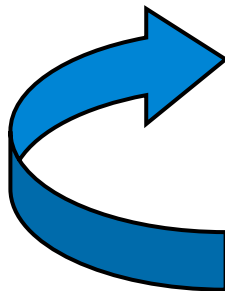


- **Healthy links transmit keep alives**

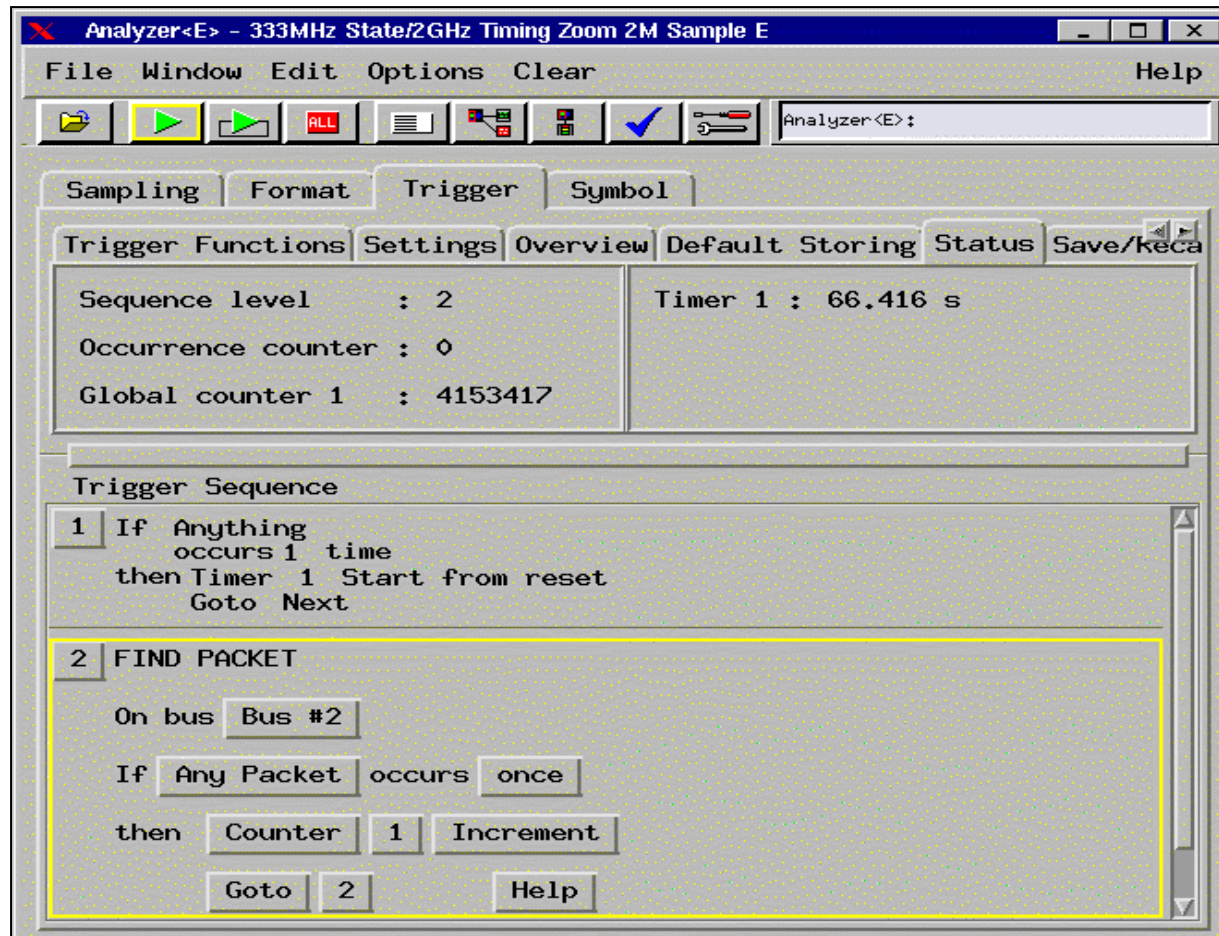


Detect Bus Inactivity – Trigger Setup

**Loop as long
as packets
occur every
100 msec**



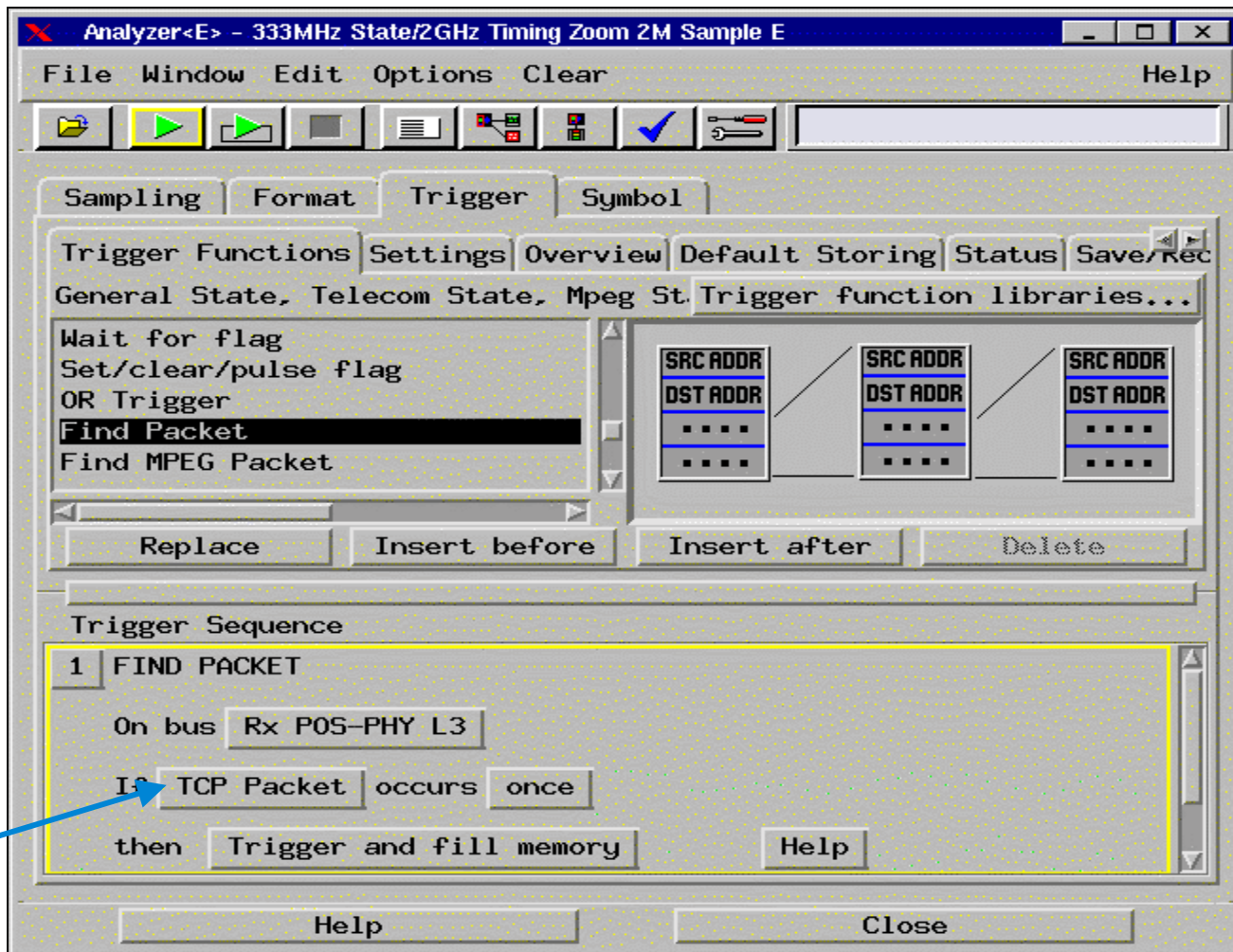
Measure Packet Throughput



- **Packets/second = 4153417/66.416**



Trigger on Specific Header Fields



Event



Packet Trigger Bus Editor

Bus Editor: Rx POS-PHY L3

Bus Name: Rx POS-PHY L3

Data Source: Analyzer<E>

Protocol: Point-to-Point Protocol (PPP)

Start of Packet/Cell: RSOP = 1 ↓ (optional)

End of Packet: REOP = 1 ↓ (optional)

Data Valid: RVAL = 1 ↓ (optional)

TSX/RSX: RSX (optional, for POS-PHY)

PHY/Address: None (optional)

Parity: RPRTY = Even ↓ (optional)

Modulo: None (optional, POS-PHY RMOD/TMOD)

Data Bus: RDAT

OK Cancel



Packet Trigger Event Editor

Event Editor: TCP Packet

Event Name: ☒ Long Field Names

Protocol Stack

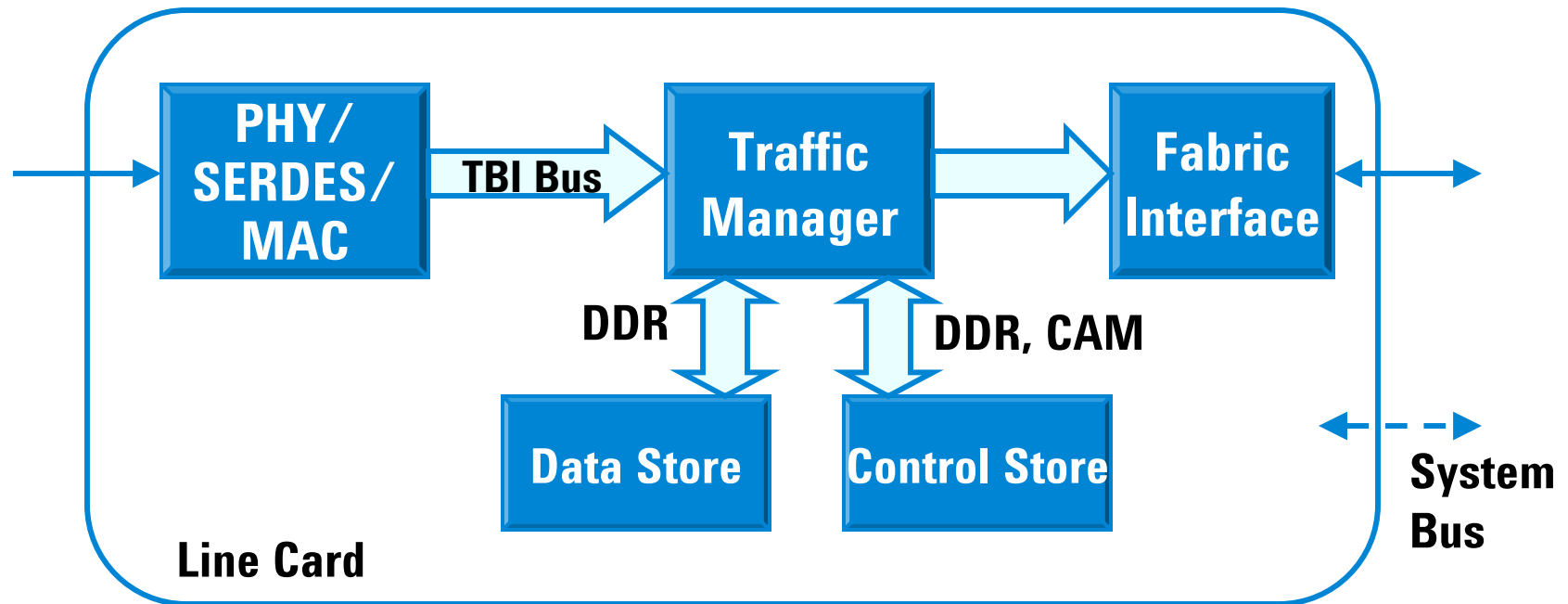
- Transmission Control Protocol
- Internet Protocol
- Point-to-Point Protocol (PPP)

Internet Protocol

Identification	<input type="text" value="XXXX"/>
Zero	<input type="text" value="X"/>
Do not fragment	<input type="text" value="X"/>
May Fragment	<input type="text" value="X"/>
Fragment Offset	<input type="text" value="XXXX"/>
Time To Live	<input type="text" value="XXX"/>
Protocol	<input type="text" value="Transmission Control Protocol (0x06)"/>
Header Checksum	<input type="text" value="XXXX"/>
Src Addr	<input type="text" value="11. 22. 33. 44"/>
Dest Addr	<input type="text" value="XXX.XXX.XXX.XXX"/>



Measure Latency Between PHY & DDR

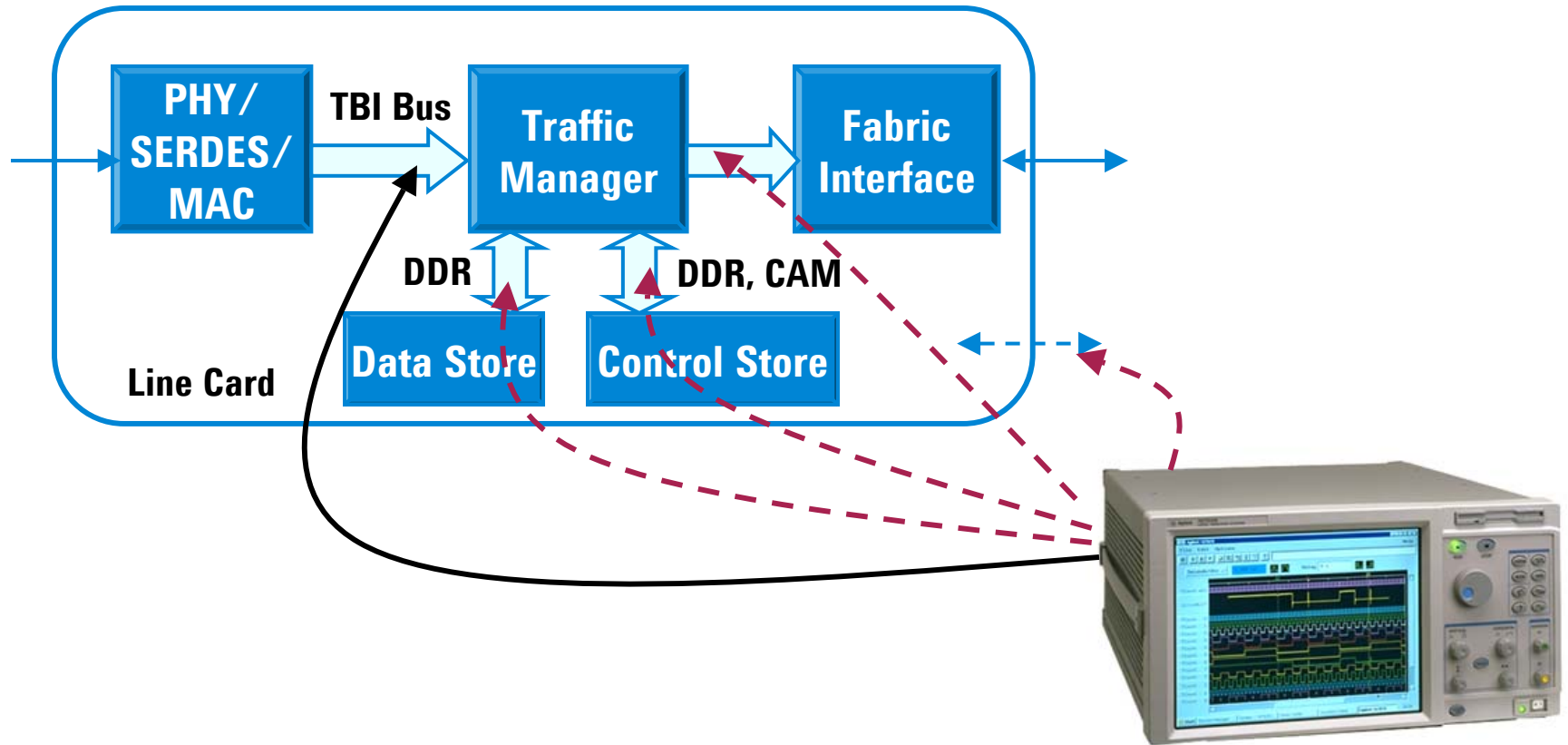


Possible causes:

1. Packets buffered in data store too long
2. Traffic manager takes too long to process
3. Route lookup goes off-board, and system board is slow to respond
4. Buffering issues causing port contention.



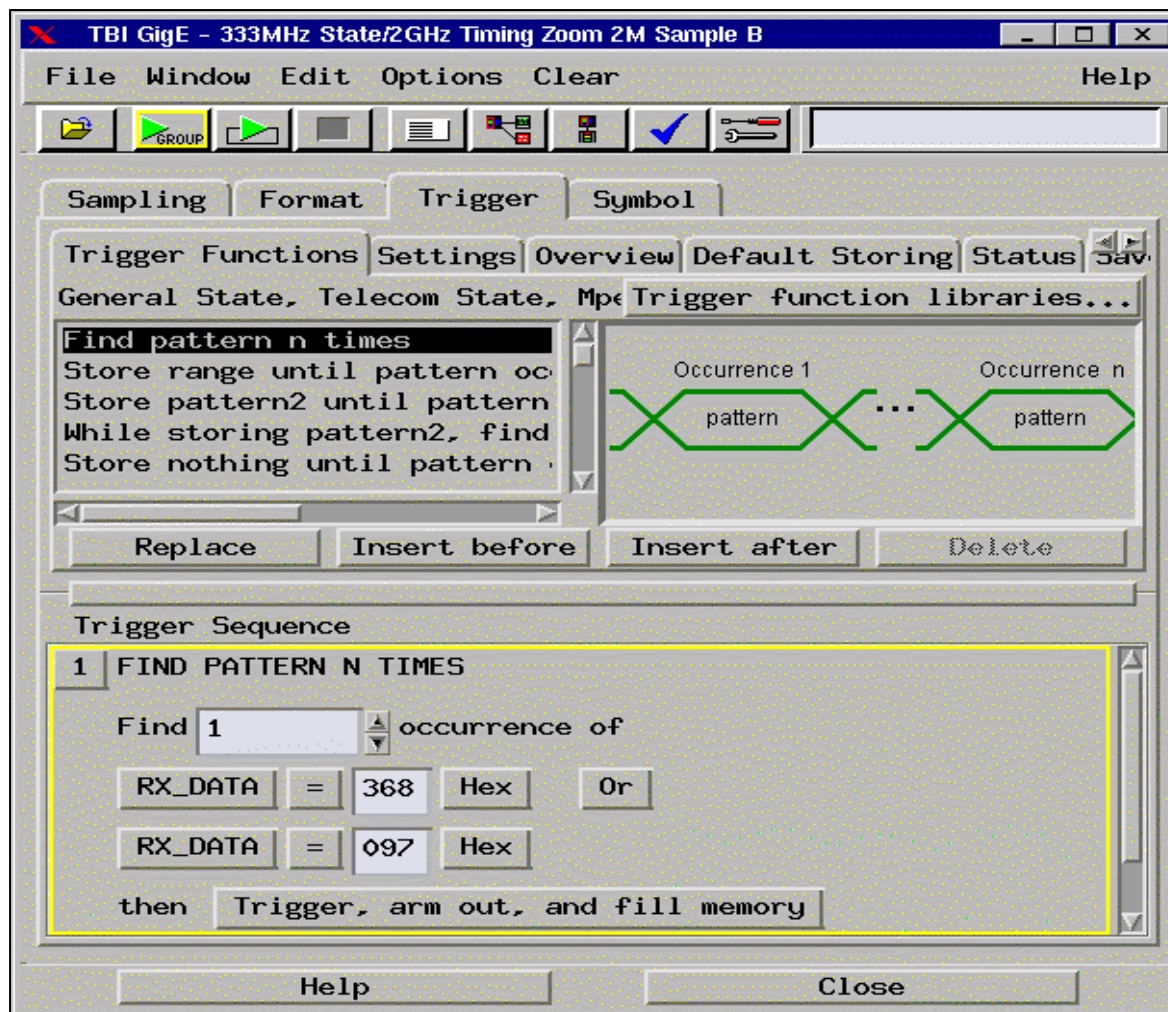
Packet Latency Between PHY & DDR



1. Trigger on Start of Packet
2. Use Intermodule trigger to correlate data store activity



TBI Bus Trigger



Data Store Bus Trigger

The screenshot displays two windows from the Agilent Data Store Bus Trigger software. The main window, titled "DataStore1 - 333MHz State/2GHz Timing Zoom 2M Sample B", features a menu bar (File, Window, Edit, Options, Clear, Help) and a toolbar. Below the toolbar are tabs for "Sampling", "Format", "Trigger", and "Symbol". The "Trigger" tab is active, showing a "Trigger Functions" list on the left and a "Wait for Arm IN" diagram in the center. The "Trigger Functions" list includes: "Find pattern2 n times after", "Store n samples", "Wait n external clock stat", "Wait for arm in" (highlighted), and "Wait for second analyzer t". Below this list are buttons for "Replace", "Insert before", "Insert after", and "Delete". At the bottom, a "Trigger Sequence" list shows: "1 WAIT FOR ARM IN", "Wait for arm in", and "then Trigger and fill memory". The "Intermodule Skew..." window is open in the background, showing a "Group Run Arming Tree" diagram with two green blocks labeled "B" and "E". Blue arrows point from labels "TBI Bus Analyzer" and "DDR Bus Analyzer" to these blocks respectively.

DataStore1 - 333MHz State/2GHz Timing Zoom 2M Sample B

File Window Edit Options Clear Help

GROUP

Sampling Format Trigger Symbol

Trigger Functions Settings Overview Default Storing Status

General State, Telecom State, Trigger function libraries...

Find pattern2 n times after
Store n samples
Wait n external clock stat
Wait for arm in
Wait for second analyzer t

Replace Insert before Insert after Delete

Trigger Sequence

1 WAIT FOR ARM IN
Wait for arm in
then Trigger and fill memory

Help Close

Intermodule Skew...

File Window Help

Intermodule Skew...

Group Run Arming Tree

Group Run

TBI Bus Analyzer

DDR Bus Analyzer



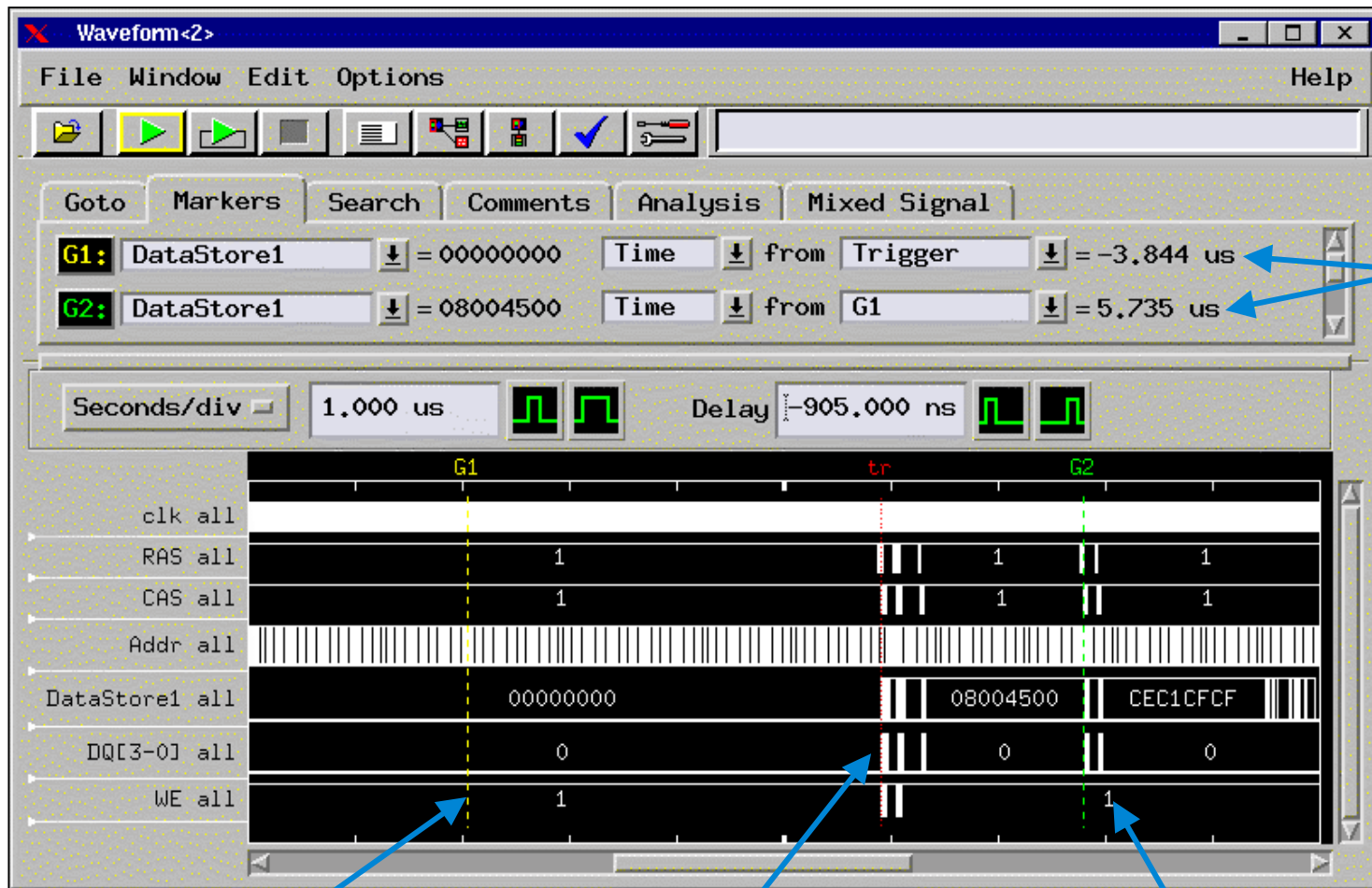
TBI Bus Decode Listing

Start of Packet →

TBI GigE List							
File Window Edit Options Invasm Source Help							
Time	RX_DATA	Char Name	8bit Data	Packet Decode	BadFCS	BadDispa	
Relative	Hex	Text	Hex	Text	Binary	Binary	
8,000 ns	245	D31,7	50	Idle	0	0	
8,000 ns	368	K27,7	FF	Start of Packet (SOP)	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	245	D21,2	55	Preamble	0	0	
8,000 ns	246	D21,6	D5	End of Preamble	0	0	
8,000 ns	274	D 0,0	00	IEEE 802.3 (Ethernet V2)	0	0	
				Dest Addr = 00-e0-00-00-00-41			
8,000 ns	271	D 0,7	E0		0	0	
8,000 ns	274	D 0,0	00		0	0	
8,000 ns	274	D 0,0	00		0	0	
8,000 ns	274	D 0,0	00		0	0	
8,000 ns	105	D 1,2	41		0	0	
8,000 ns	075	D31,7	47	Src Addr = 47-49-4c-45-4e-54	0	0	
8,000 ns	255	D 9,2	49		0	0	
8,000 ns	005	D12,2	4C		0	0	
8,000 ns	295	D 5,2	45		0	0	
8,000 ns	105	D14,2	4E		0	0	
8,000 ns	0B5	D20,2	54		0	0	
8,000 ns	06B	D31,7	08	Length/Type = 0800 Hex (Internet Protocol)	0	0	
8,000 ns	18B	D31,7	00		0	0	
8,000 ns	295	D 5,2	45	Internet Protocol	0	0	
				Version = 4 Hex			
				Header Length = 5 Decimal			



DDR Data Store Timing Waveform



Easy
marker
measure-
ments

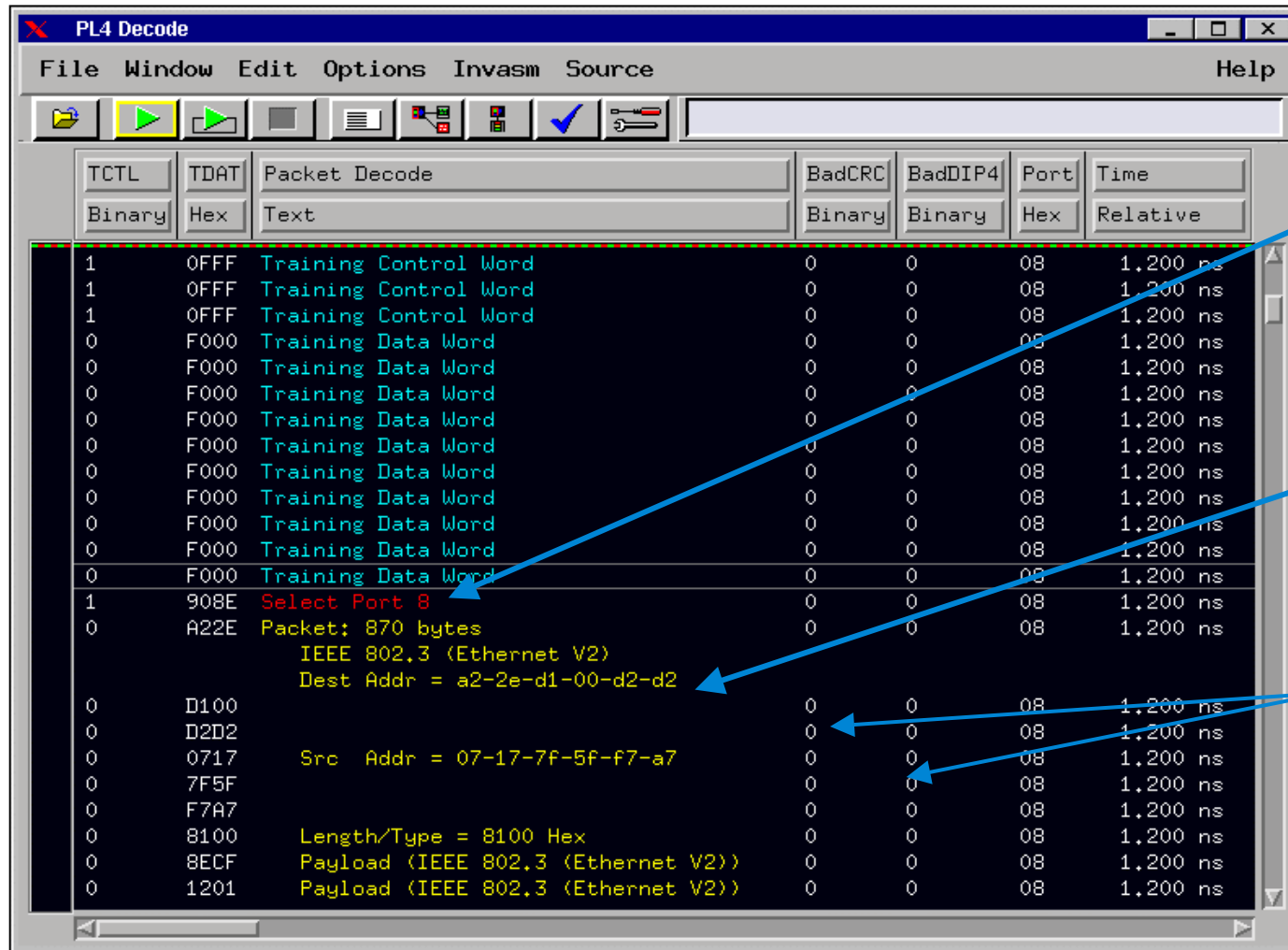
Packet arrives on
Receive TBI Bus

Packet written to data
store 3.8 usec later

Packet read back
out of Data Store



POS-PHY Level 4 Analysis



TCTL	TDAT	Packet Decode	BadCRC	BadDIP4	Port	Time
Binary	Hex	Text	Binary	Binary	Hex	Relative
1	0FFF	Training Control Word	0	0	08	1,200 ns
1	0FFF	Training Control Word	0	0	08	1,200 ns
1	0FFF	Training Control Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
0	F000	Training Data Word	0	0	08	1,200 ns
1	908E	Select Port 8	0	0	08	1,200 ns
0	A22E	Packet: 870 bytes	0	0	08	1,200 ns
		IEEE 802.3 (Ethernet V2)				
		Dest Addr = a2-2e-d1-00-d2-d2				
0	D100		0	0	08	1,200 ns
0	D2D2		0	0	08	1,200 ns
0	0717	Src Addr = 07-17-7f-5f-f7-a7	0	0	08	1,200 ns
0	7F5F		0	0	08	1,200 ns
0	F7A7		0	0	08	1,200 ns
0	8100	Length/Type = 8100 Hex	0	0	08	1,200 ns
0	8ECF	Payload (IEEE 802.3 (Ethernet V2))	0	0	08	1,200 ns
0	1201	Payload (IEEE 802.3 (Ethernet V2))	0	0	08	1,200 ns

Reassemble packets from multi-port operation

Decode the PPP and TCP/IP stacks

Check DIP-4 Parity and CRC Codes



PHY Transmit/Receive Latency

Sampling Format **Trigger** Symbol

Trigger Functions Settings Overview Default Storing Status Save/Recall

Sequence level : 1	Timer 1 : 0
Occurrence counter : 0	
Global counter 1 : 0	

Trigger Sequence

1 FIND PACKET

On bus Rx Bus

If ARP Request occurs once

then Timer 1 Resume

Goto Next Help

2 FIND PACKET

On bus Tx Bus

If ARP Response occurs once

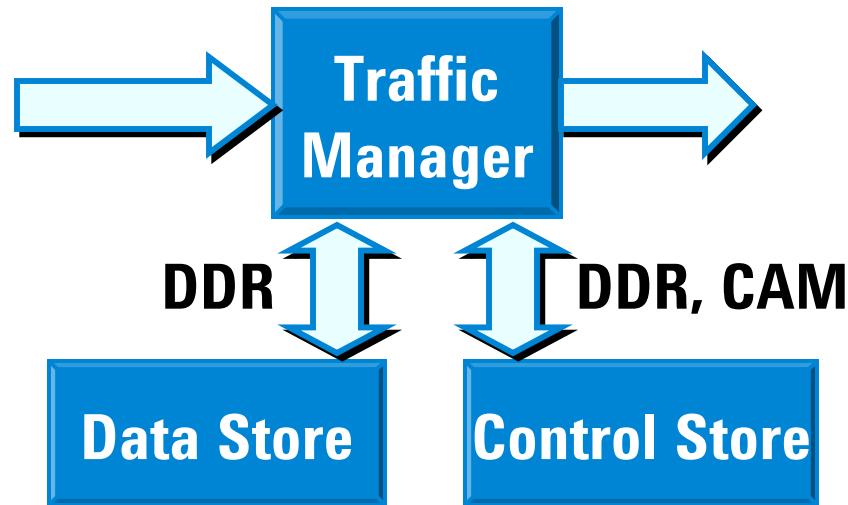
then Timer 1 Pause

Counter 1 Increment

Goto 1



Find Cause of Dropped Packets



Possible Trigger Schemes:

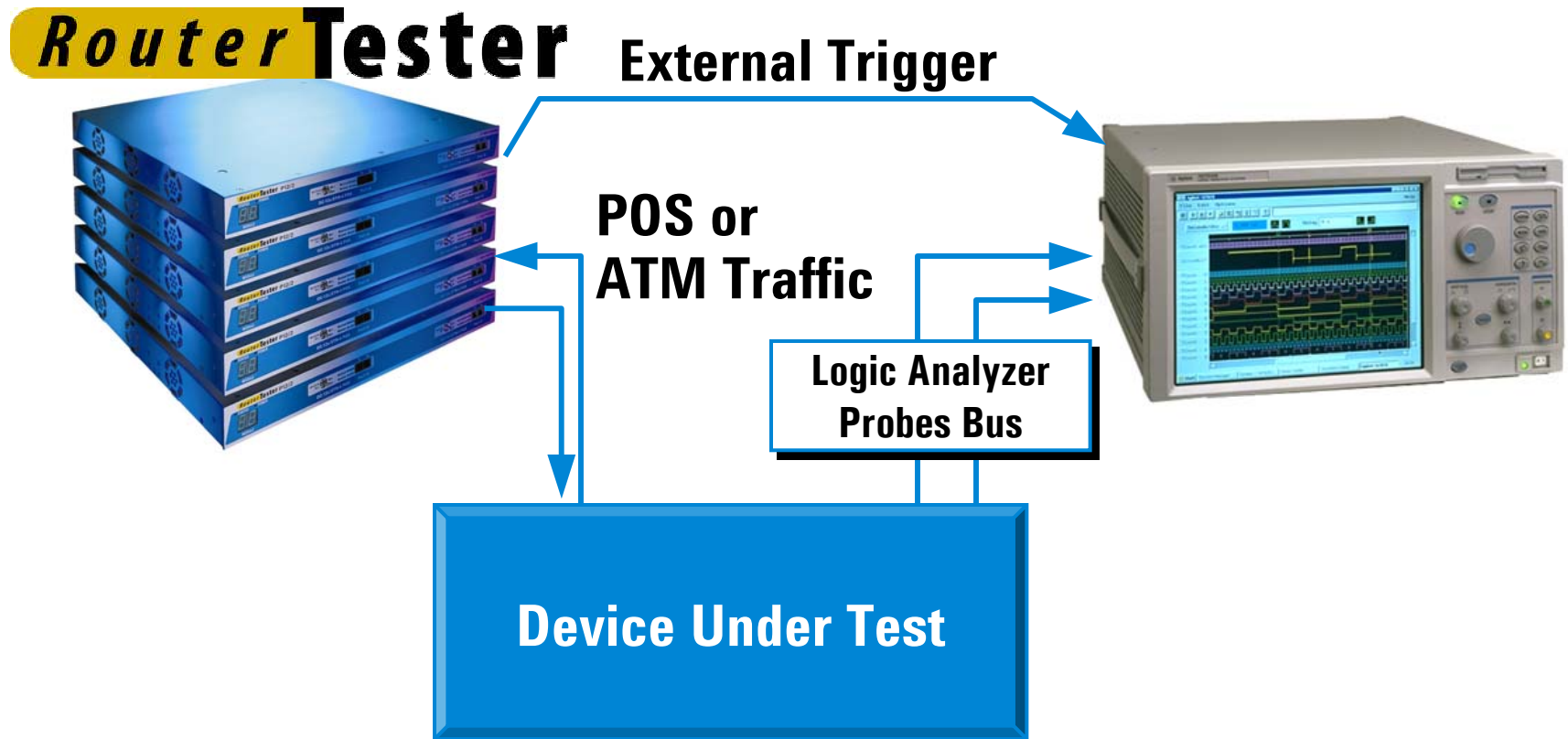
- Address out of range in data store
- Signals indicating queue getting full
- Debug port on network processor

Possible causes:

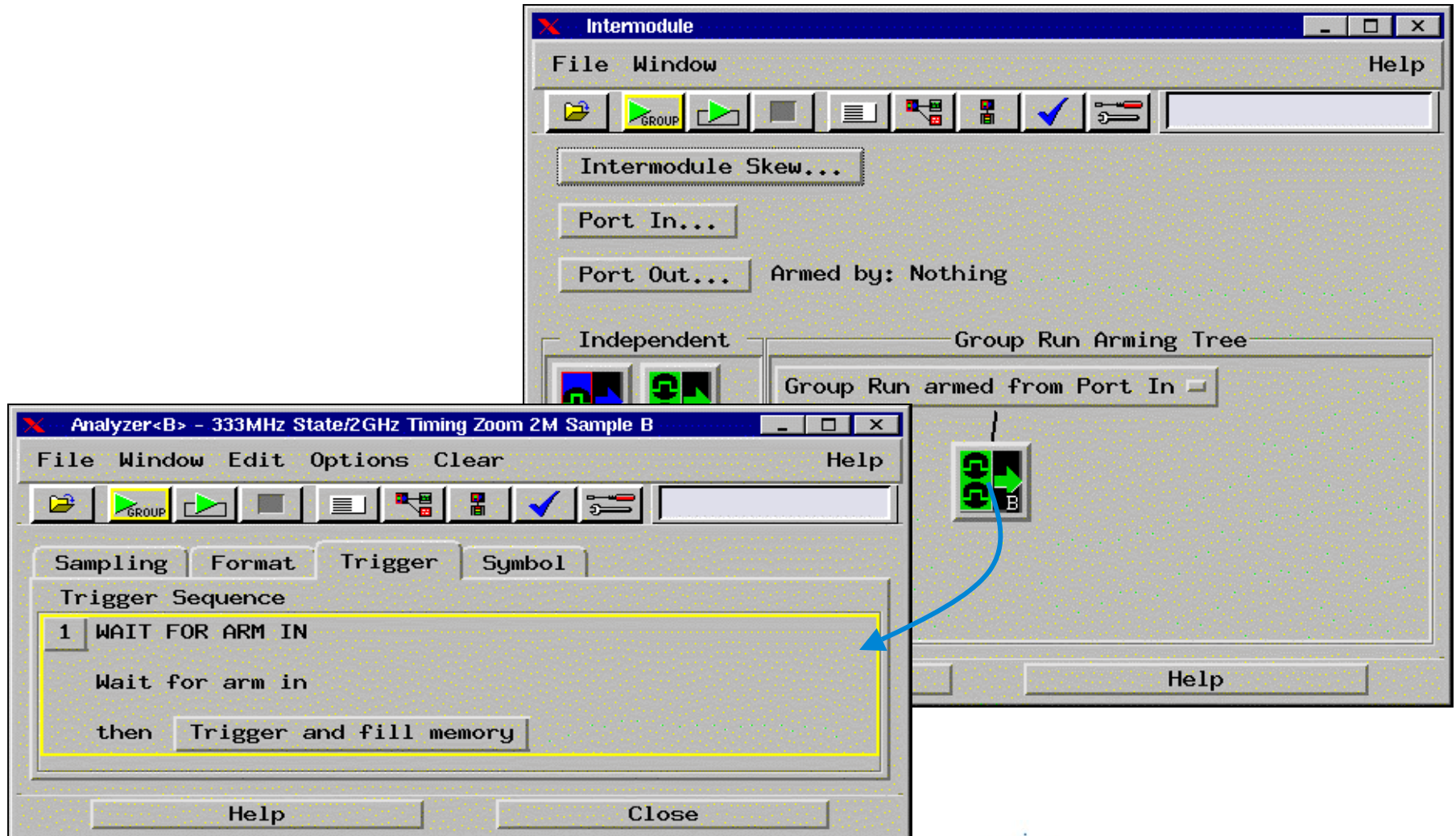
- Latencies in route lookups
- Too much high-priority traffic
- Too many short packets
- Firmware/logic bugs in scheduling



Strategy - External Trigger Sources



External Trigger – Analyzer Setup



Protocol Decoding and Triggering

Bus	Protocol(s)	Packet Trigger	Decode Software	Product
UTOPIA L1-3	ATM, Cells and AAL5	Yes	Yes	B4640B
POS-PHY-L3	POS, Ethernet	Yes	Yes	B4640B
POS-PHY L4 (SPI-4 Phase 2)	OC-192 POS, 10 G Ethernet	No	Yes	N4214A
MII, GMII	Ethernet, other non-segmented	Yes	Yes	B4640B
TBI (Gbit Ethernet)	Ethernet, or other non-segmented	No (8B/10B encoded)	Yes	N4212A
InfiniBand	SERDES 10-bit interface or cable	Yes (via N4207A analysis probe)	Yes	N4206A N4207A



Capture-only Buses

HyperTransport (LDT)	16760 (Solution coming from FuturePlus)
Rapid/I/O	16760 (Decode tool coming soon)
CSIX	1675X

Note - Packet trigger macro not available on 16760 in high-speed LVDS mode



Conclusion

- **Troubleshooting bleeding-edge systems is critical**
- **Systems must be designed for testability**
- **Logic analysis tools are essential for router debug**
 - **Probe LVDS signals**
 - **Trigger on packets**
 - **View decoded protocols**

For more information see the R&D Central Website:

<http://www.agilent.com/find/randd>

- **Discussion forums**
- **Application notes**

